

Janus Schematic Beema

2014-03-05

REV : A00

DY : None Installed

UMA: UMA only installed

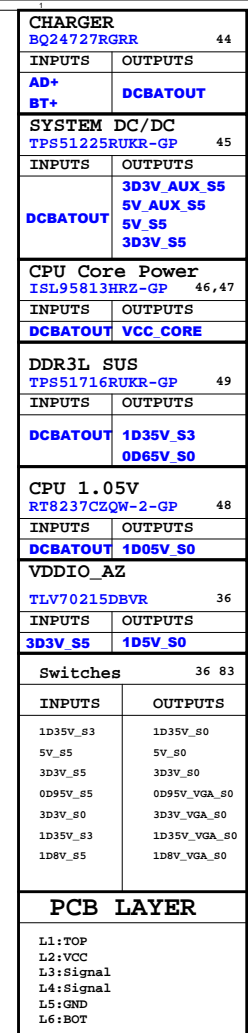
OPS: DISCRTE SG installed

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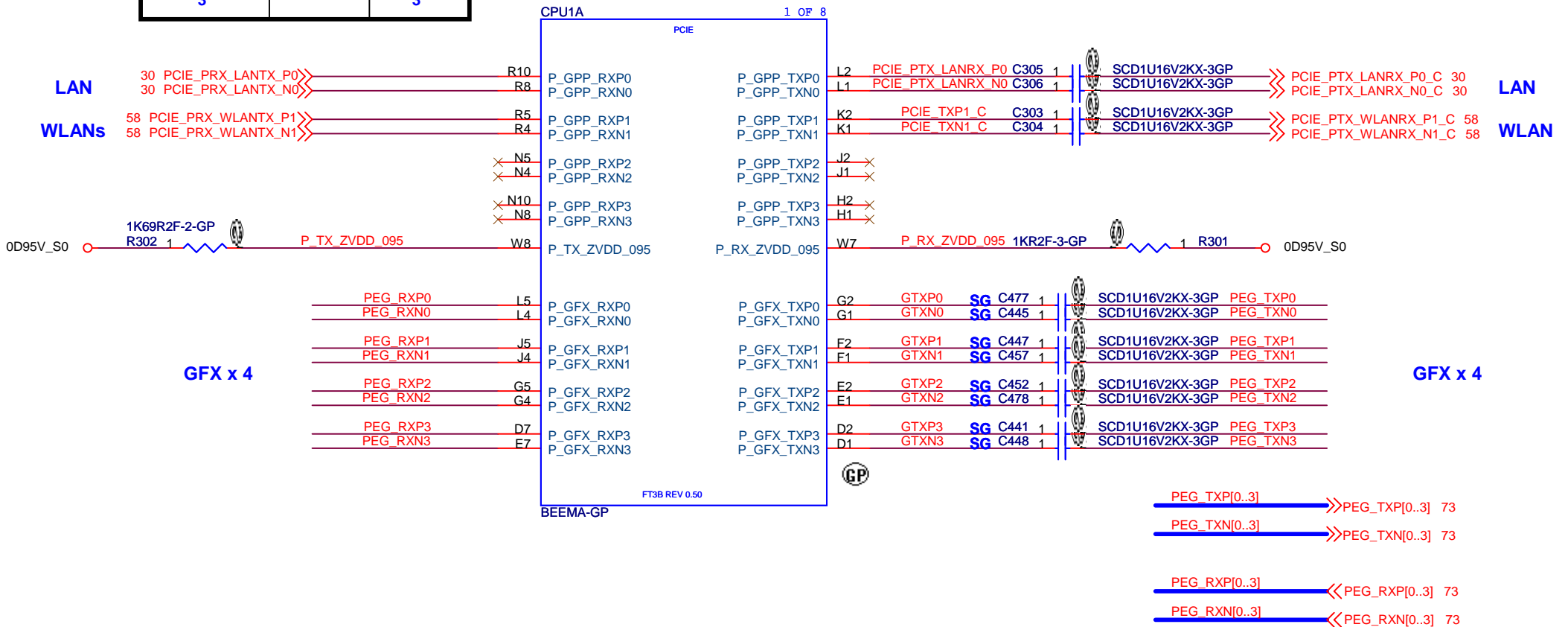
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Title			
Cover Page			
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Janus Block Diagram



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GPP CLK port	Device	CLKREQ#
0	LAN WLAN	0
1		1
2		2
3		3

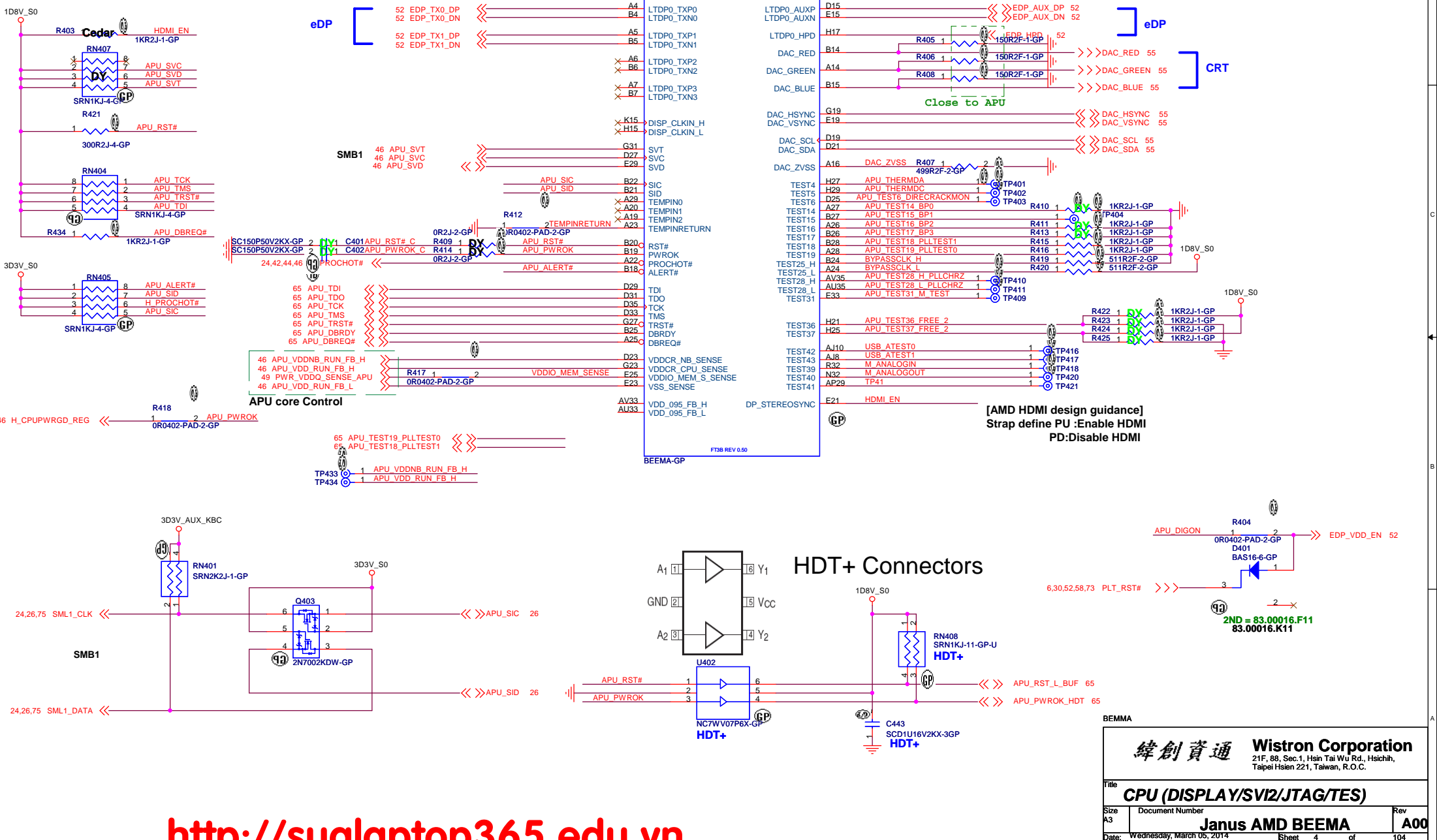


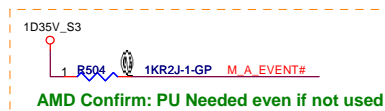
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CPU (PCIE)			
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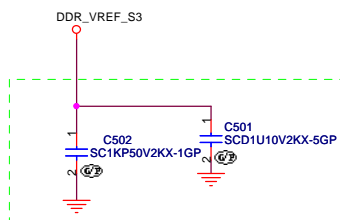
Pre-PWROK METAL VID CODES

SVD	SVC	Output Voltage
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8

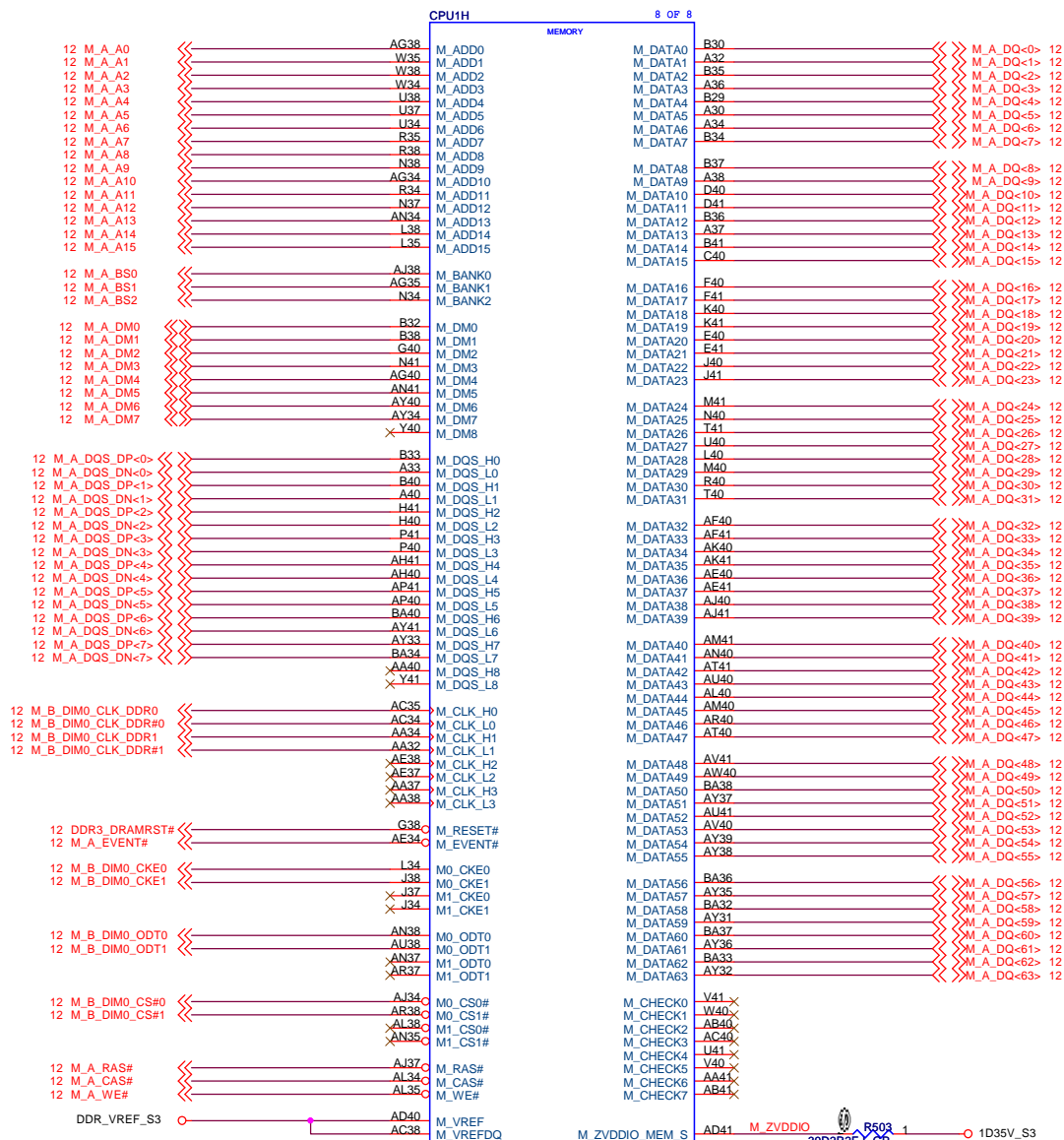




AMD Confirm: PU Needed even if not used



LAYOUT: place them close to APU



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3D3V_S0

There are integrated pull-up.

R635 1 10KR2J-3-GP BLUETOOTH_EN

R603 1 10KR2J-3-GP H_A2OGATE

R604 1 10KR2J-3-GP KB_DET#

R601 1 10KR2J-3-GP DBC_EN

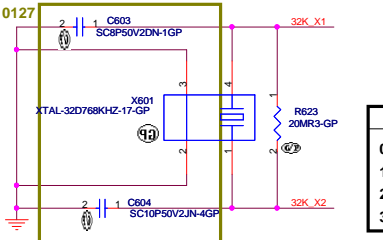
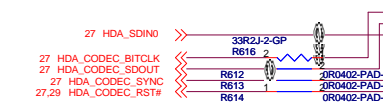
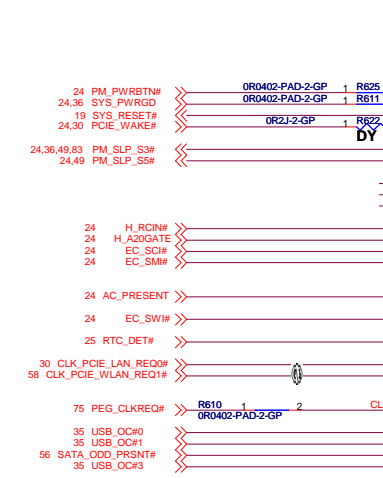
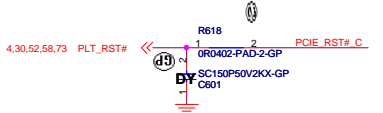
24,65 LPC_RST# << 1 2 R602 0R0402-PAD-2-GP LPC_RST#_C

CEDAR_JANUS_ID	
1	CEDAR
0	JANUS

Pin	Signal	Function
R630	10KR2J1-3-GP	PM_PWRBTN# R
R634	10KR2J1-3-GP	RTC_DET#
R617	10KR2J1-3-GP	AC_PRESENT
R626	10KR2J1-1-GP	PCIE_WAKE# R

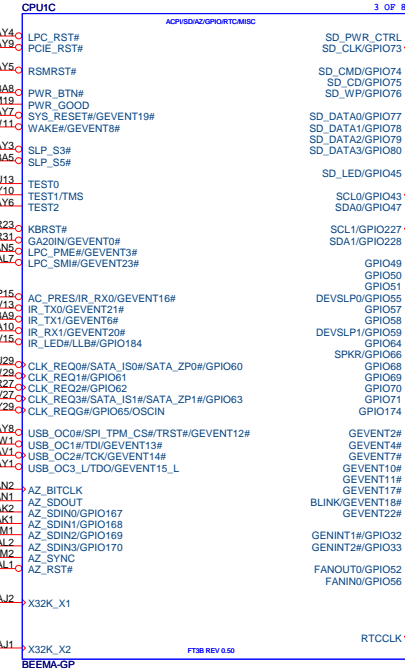
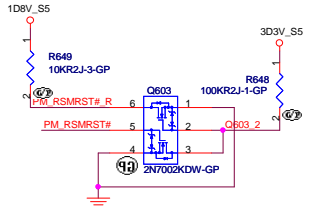
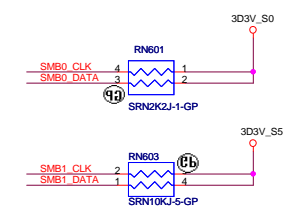
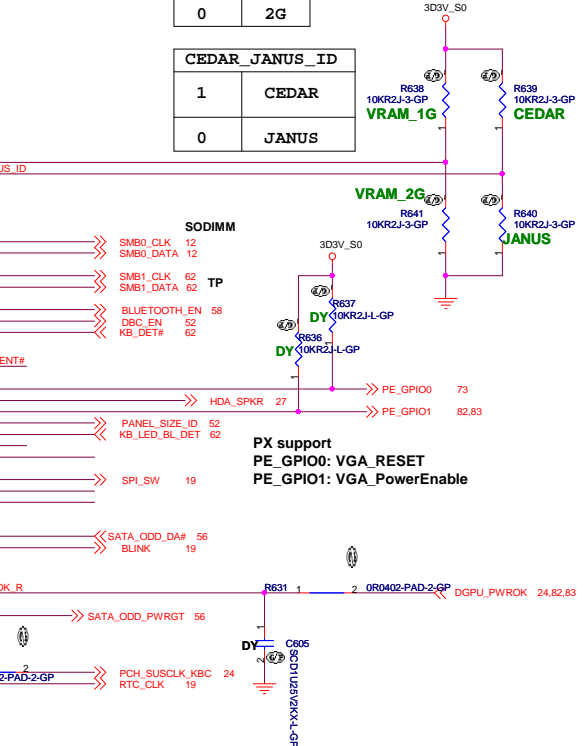
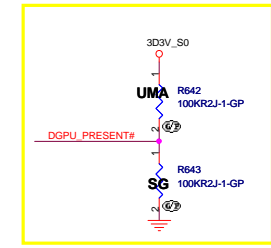
Pin	Signal	Function
RN604	8	USB_OC#1
2	6	USB_OC#3
4	5	USB_OC#0
SRN11	1-6-GP	EC_SW#

Pin	Signal	Function
R629	100KR2J1-1-GP	PM_RSMRST#
R633	10KR2J1-3-GP	HDA_SDPIN
R607	10KR2J1-3-GP	PE_GDQO
R620	10KR2J1-3-GP	GEVENT4#
R621	10KR2J1-3-GP	GEVENT7#
R647	15KR2J1-1-GP	APU_TEST0
R646	15KR2J1-1-GP	APU_TEST1
R645	15KR2J1-1-GP	APU_TEST2
R632	10KR2J1-3-GP	GPIO71
R644	10KR2J1-3-GP	MEM_1V5



	XTAL	CLK, Hz
0	System & USB	48M
1	RTC	32.768K
2	LAN	25M
3	VGA	27M

AMD suggests Xtal ESR must be less than 65R

Report APU
H=UMA L=DISCRETE

BEMM

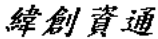
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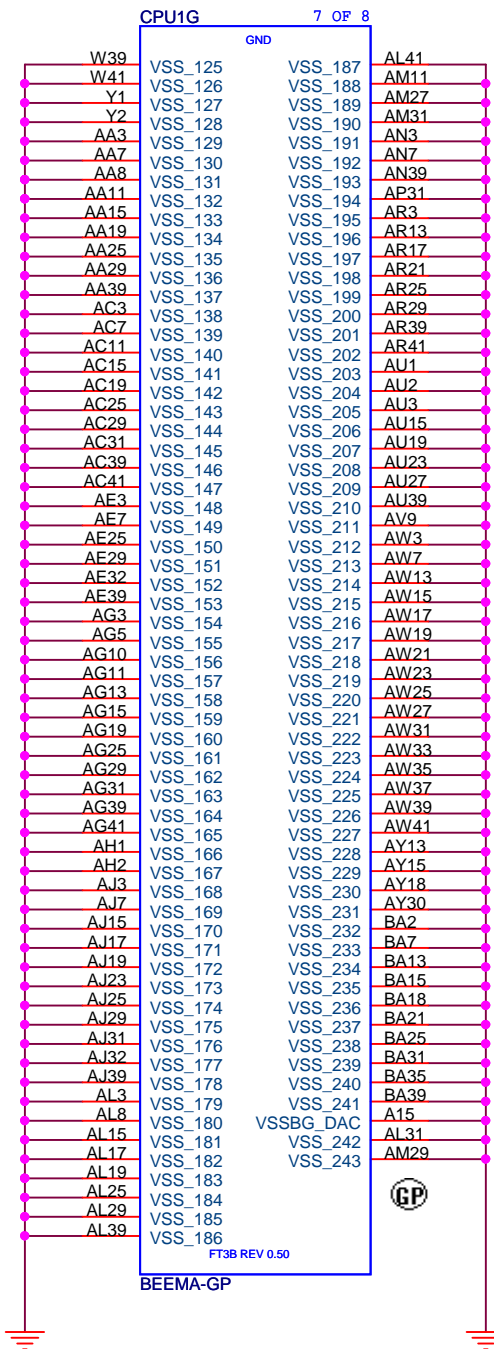
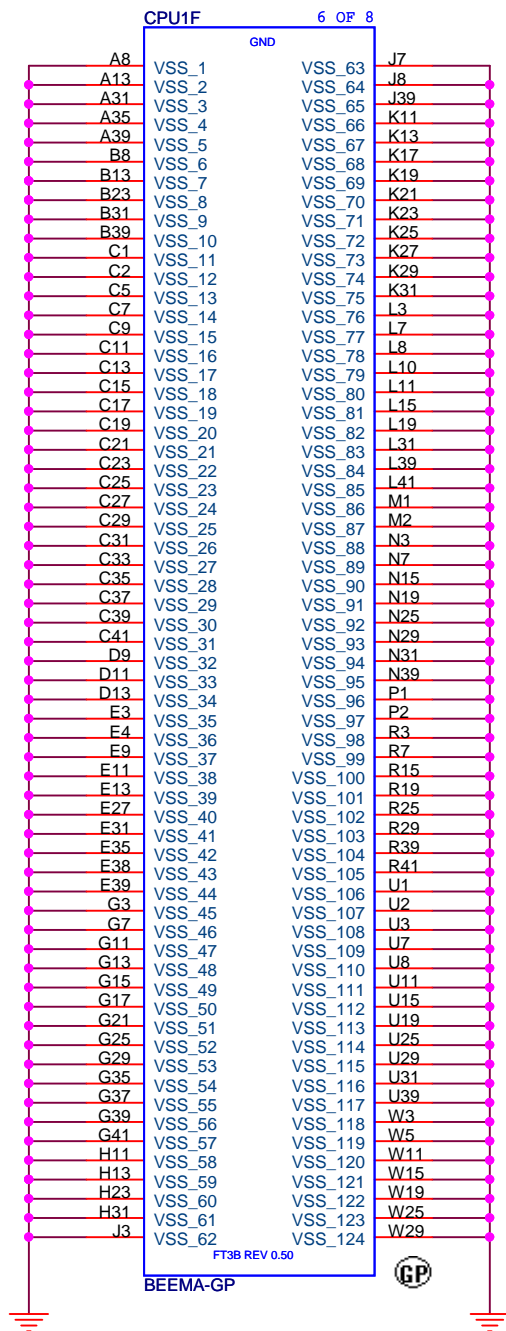
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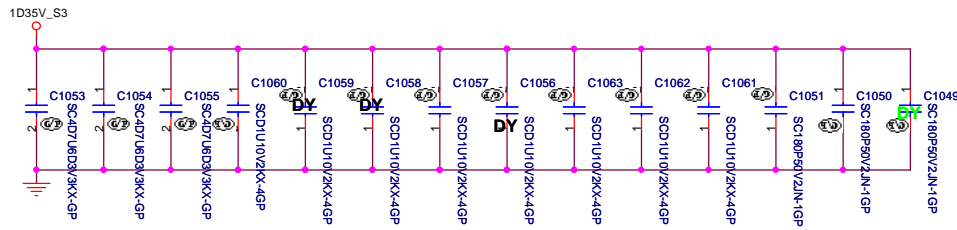
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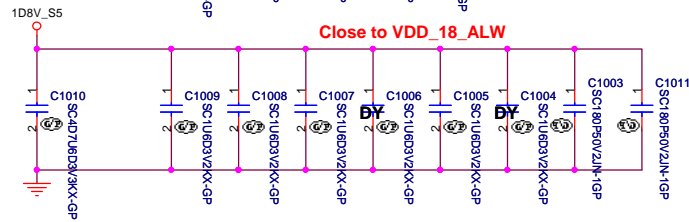
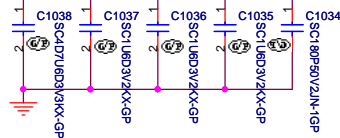
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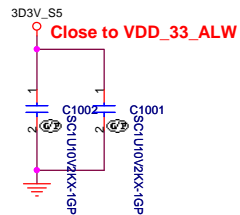
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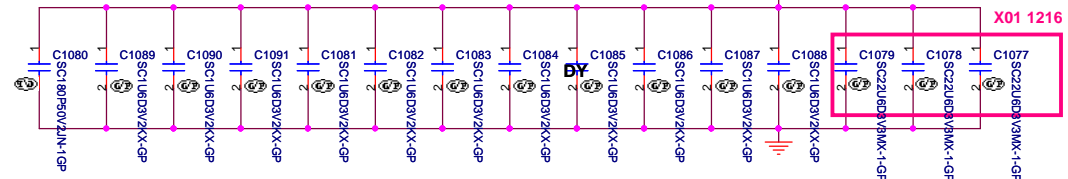
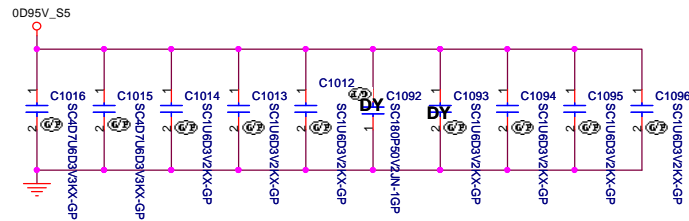
Close to VDDIO_AZ_ALW



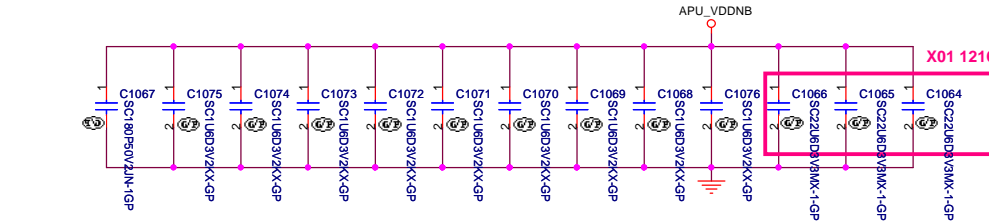
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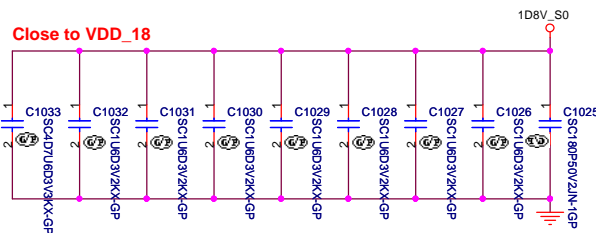
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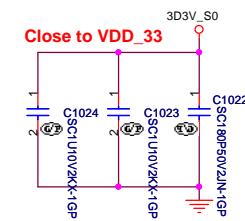
X01 1216



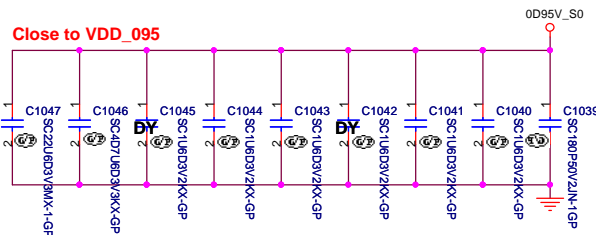
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Close to VDD_18



Close to VDD_33



Close to VDD_095

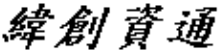
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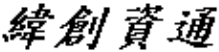
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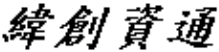
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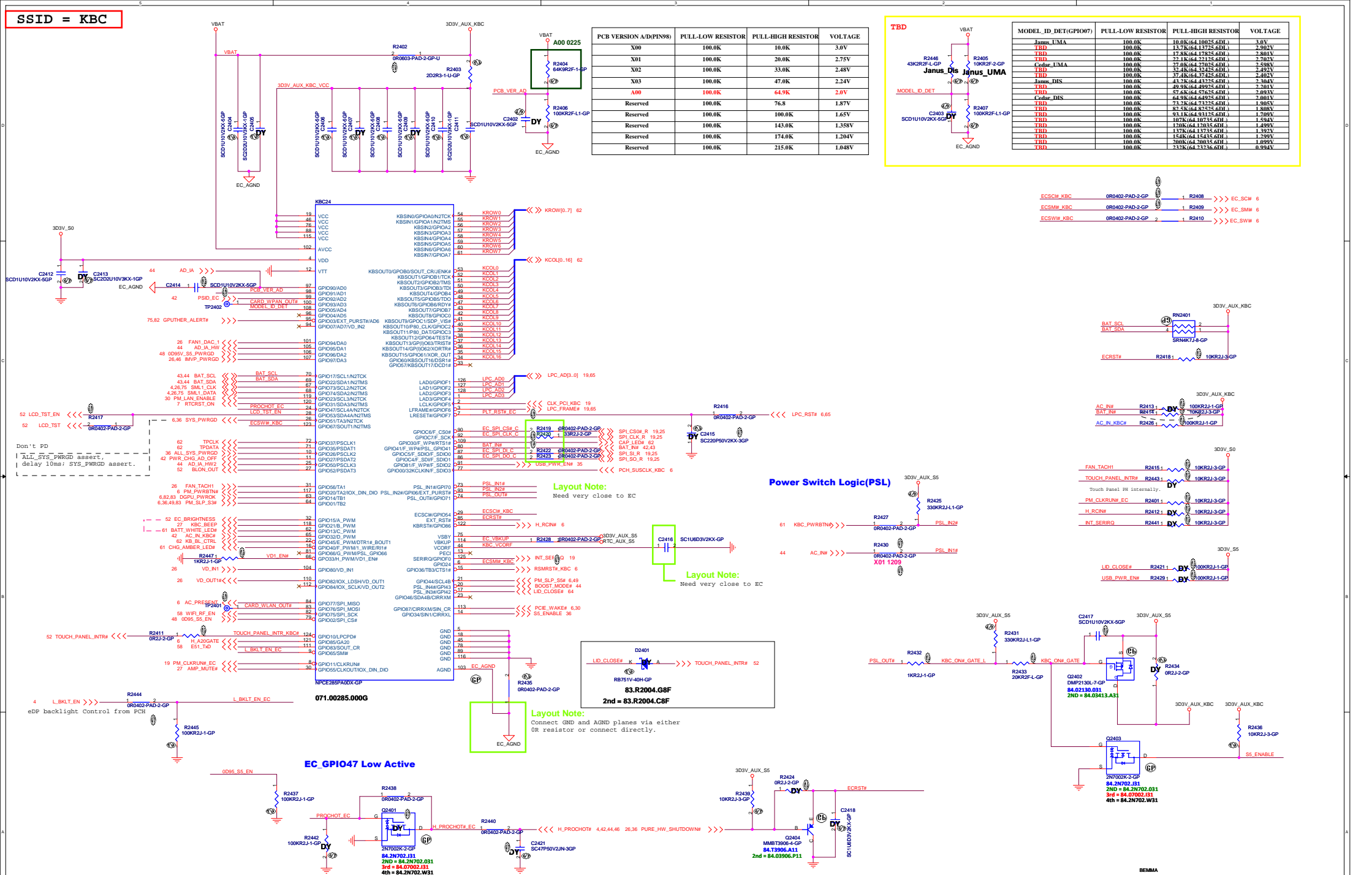
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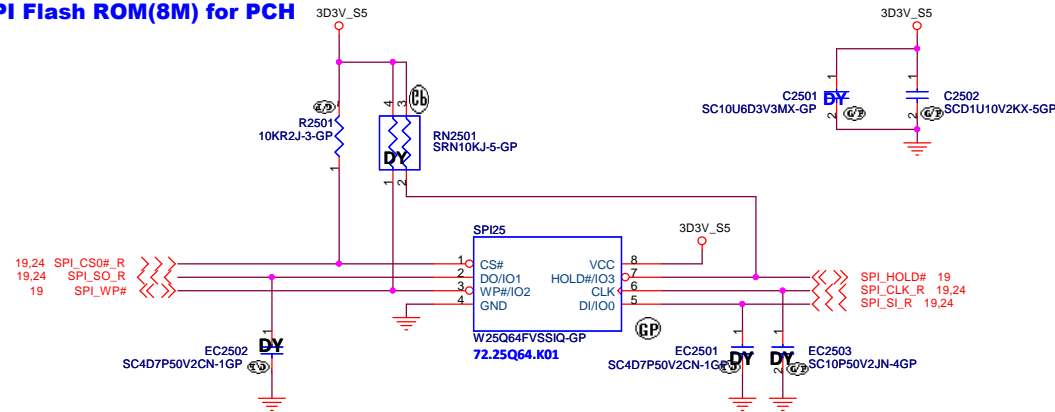
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SSID = KBC



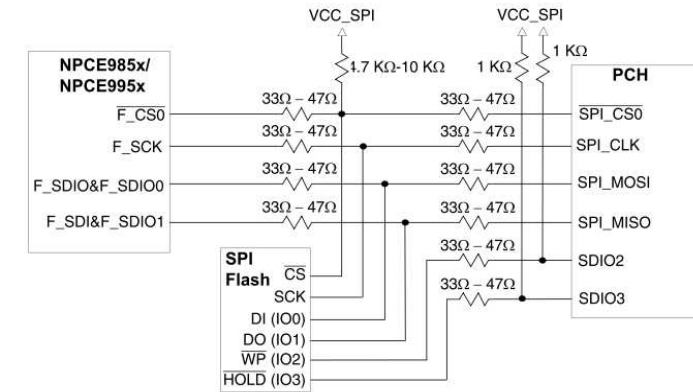
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



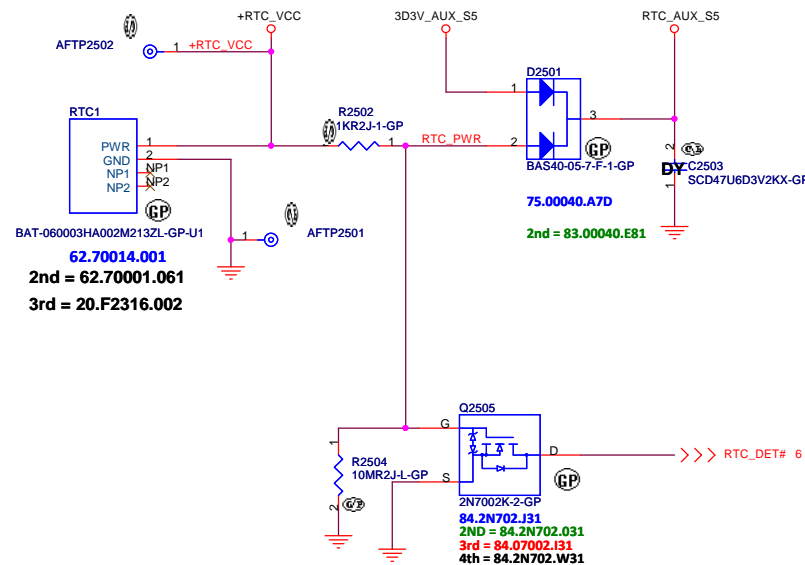
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NPCE985x/ NPCE995x board design reference guide"

SSID = RBATT



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Title	Flash/RTC	
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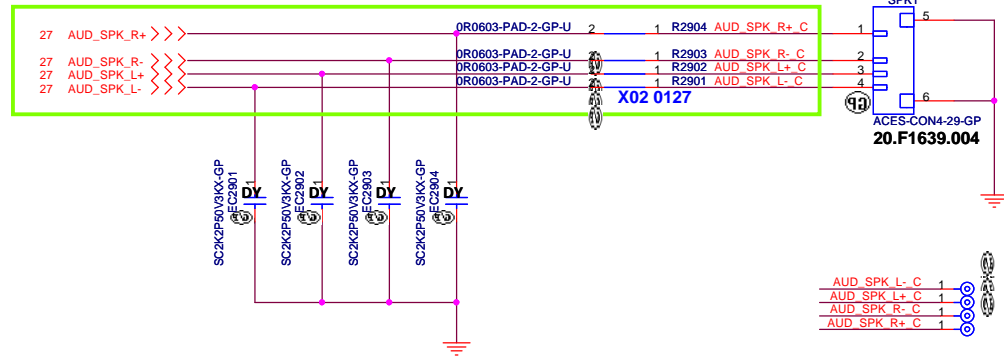
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SSID = AUDIO

Layout Note:

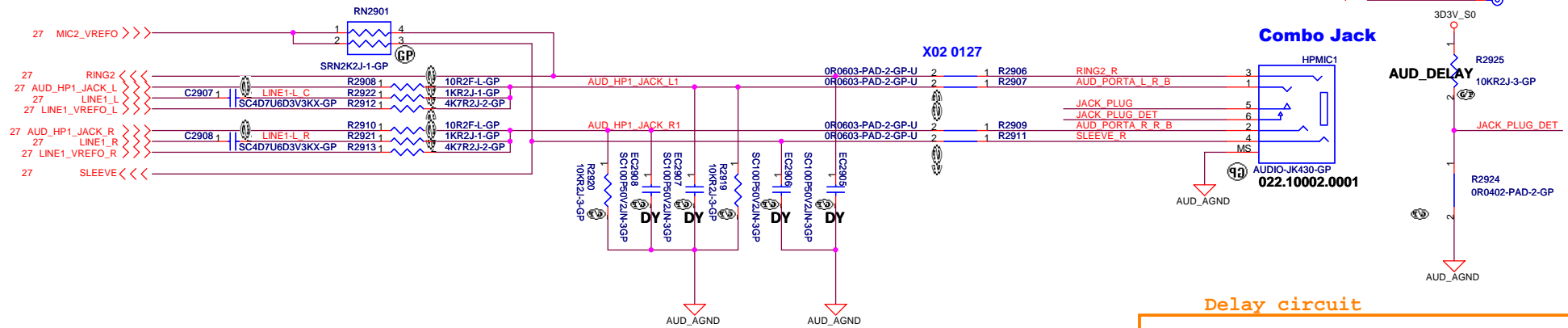
Speaker trace width >40mil @ 2W4ohm speaker power



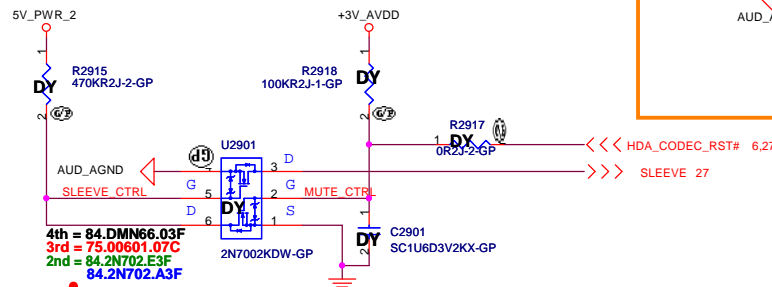
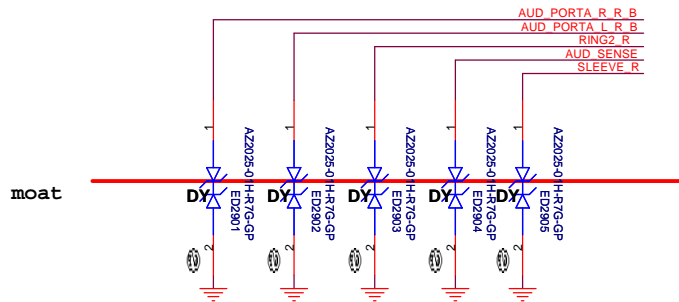
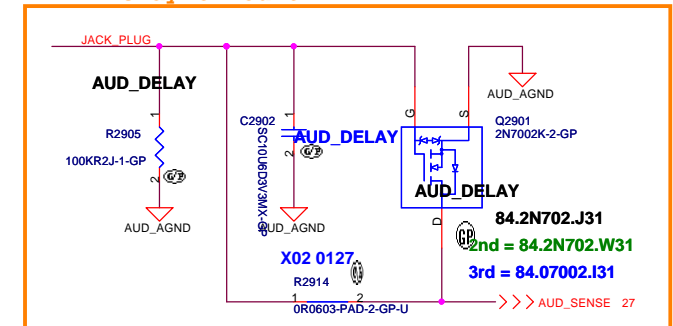
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

AUD_SPK L- C 1
AUD_SPK L+ C 1
AUD_SPK R- C 1
AUD_SPK R+ C 1

AFTP2901
AFTP2902
AFTP2903
AFTP2904



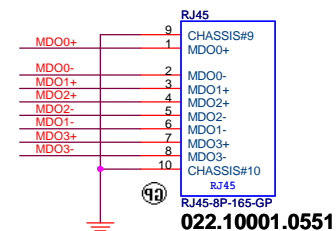
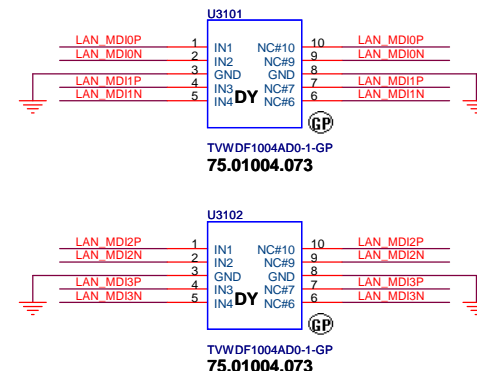
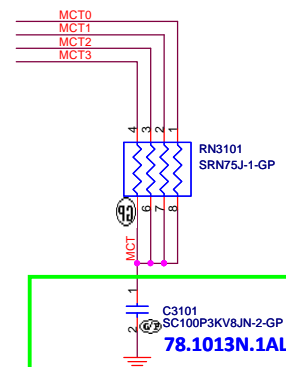
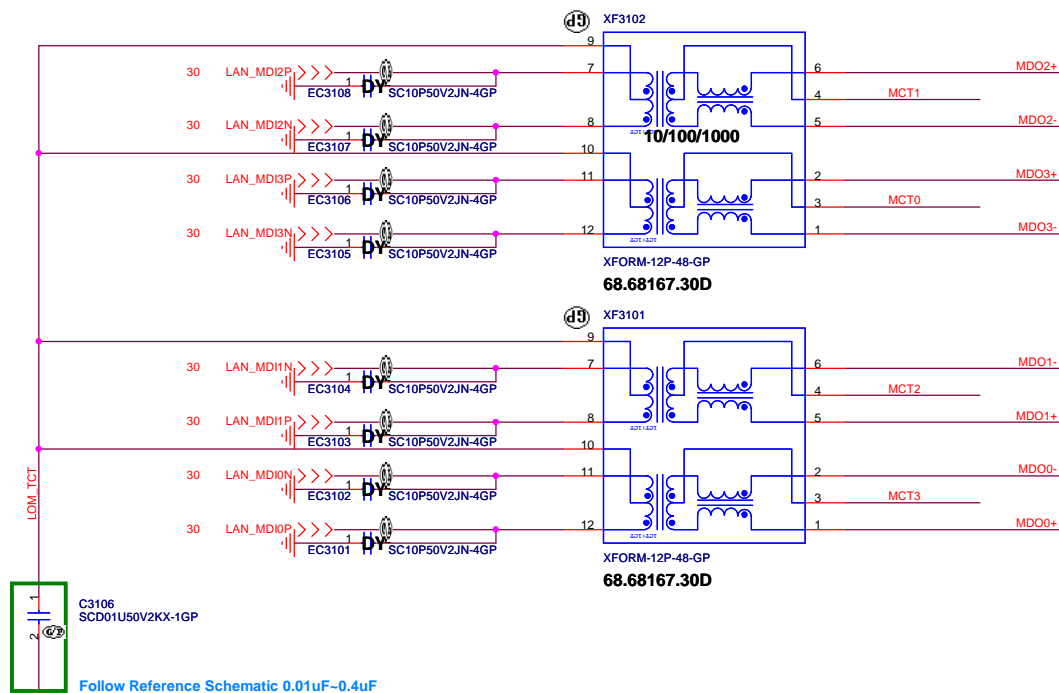
Delay circuit



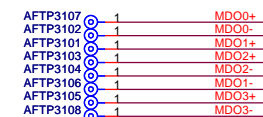
SSID = LOM

LAN TransFormer (10/100/1000M & 10/100M co-lay)

Layout note:
30 mil spacing between MDI differential pairs.



Layout:
Place near RJ45



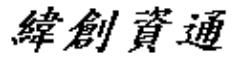
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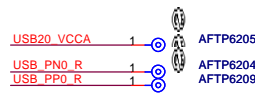
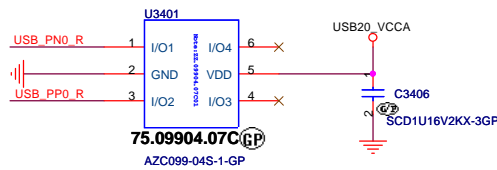
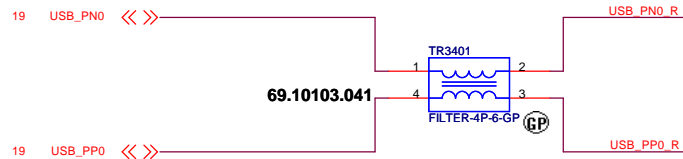
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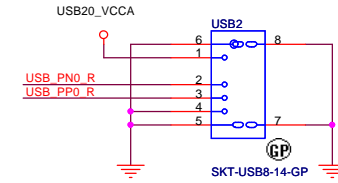
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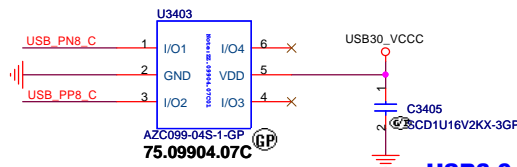
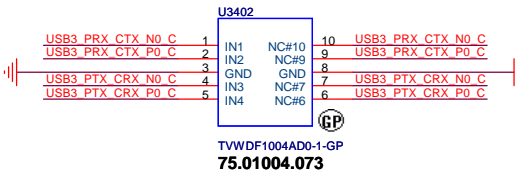
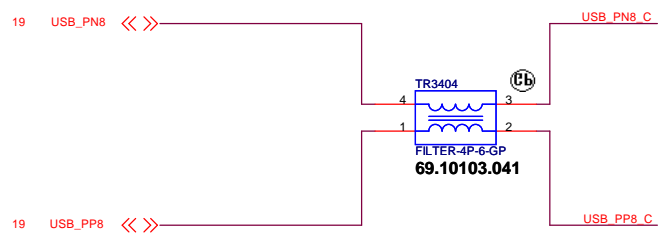
SSID = USB



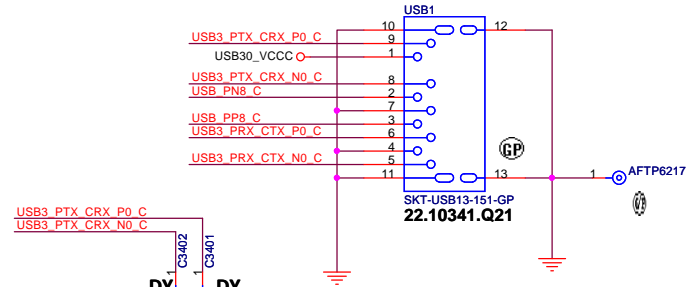
USB2.0 Port2



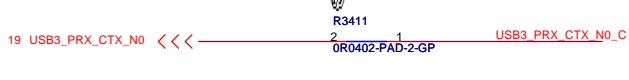
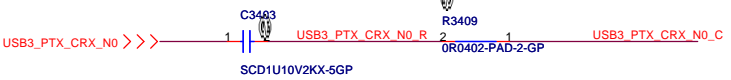
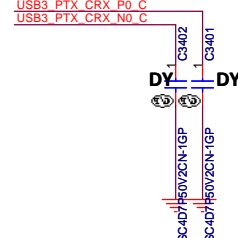
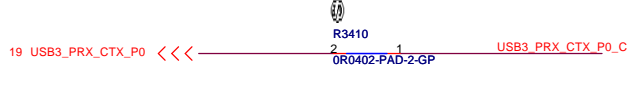
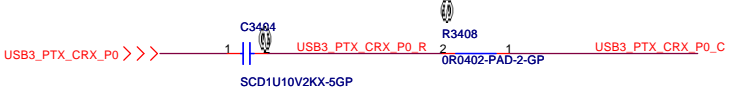
22.10321.E91



USB3.0 Port1



22.10341.Q21



BEEMA

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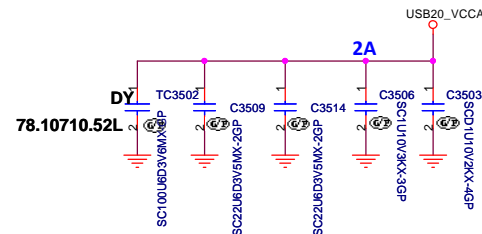
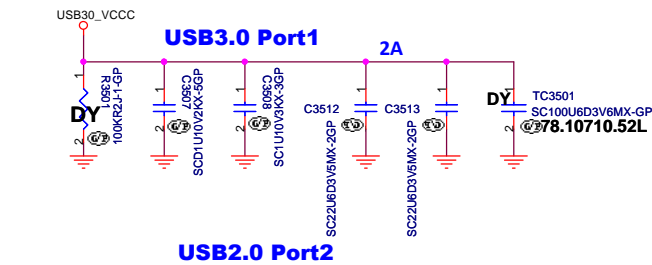
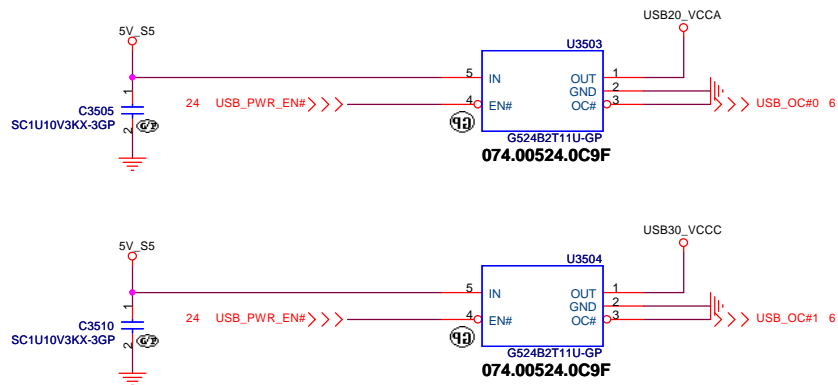
Title

USB 3.0

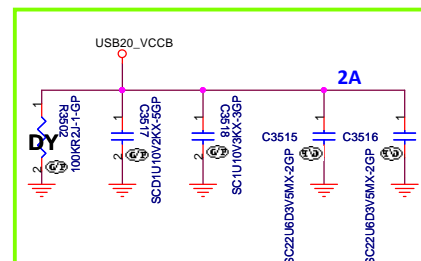
Size A3 Document Number **Janus AMD BEEMA** Rev **A00**

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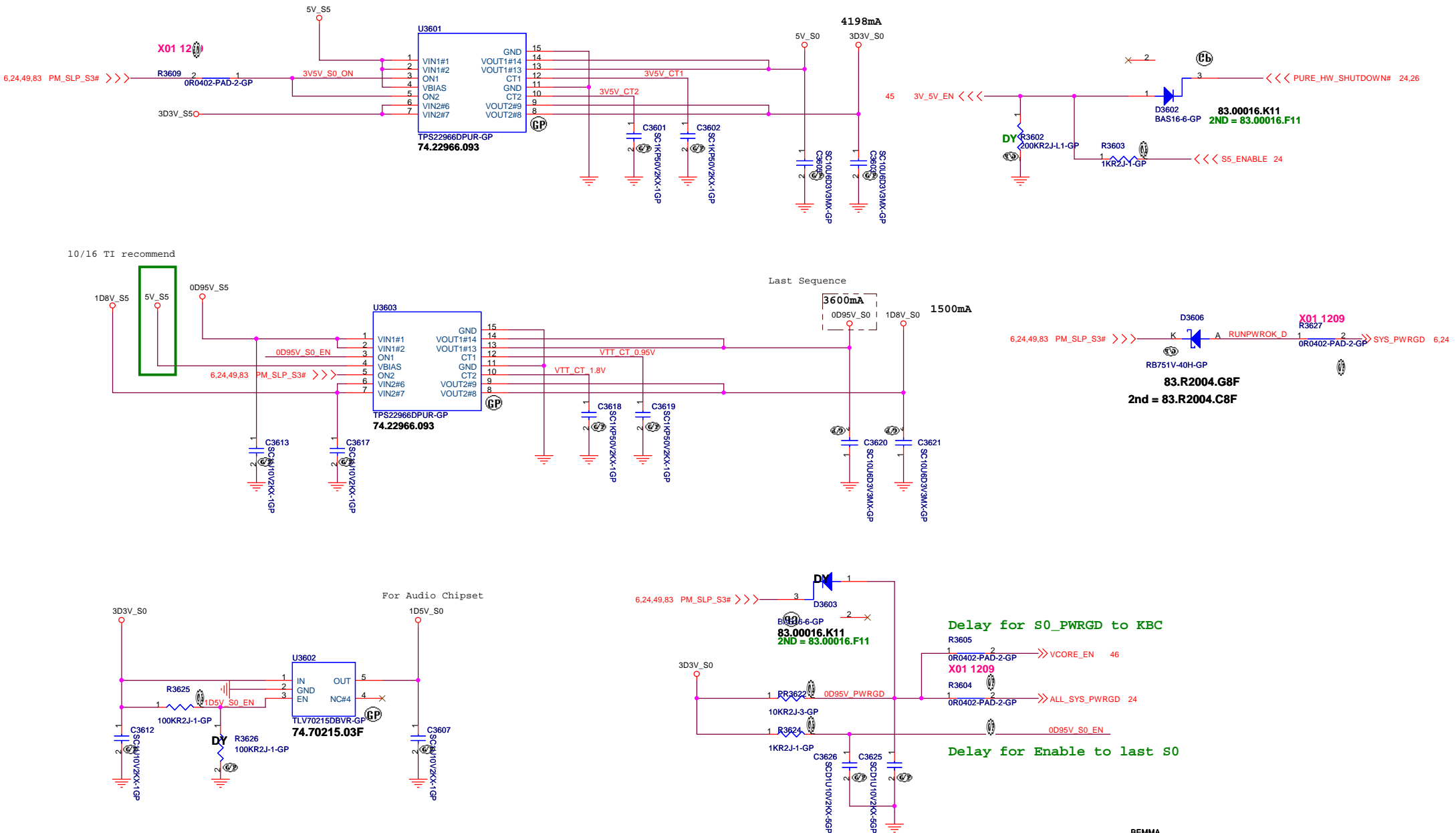
Layout Note: Close CON1



USB2.0 Port3 (IO Board)

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Power Sequence



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Title		
Power Plane Enable		
Size A3	Document Number	Rev
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SSID = Reset.Suspend

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BEMMA		
<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title (Reserved)		
Size A4	Document Number Janus AMD BEEMA	Rev A00
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Title

(Reserved) 1D05_M

Size
A4

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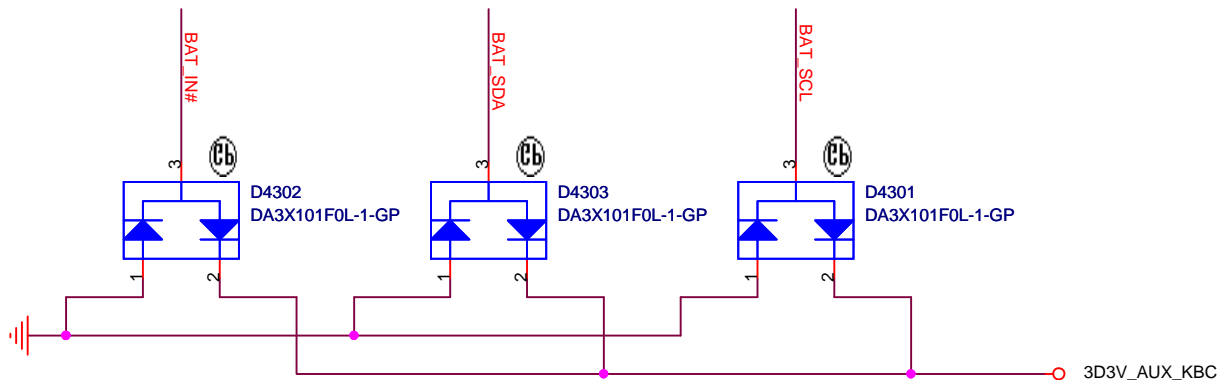
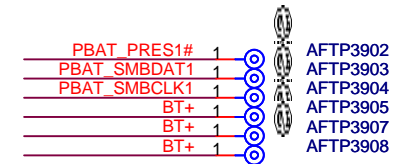
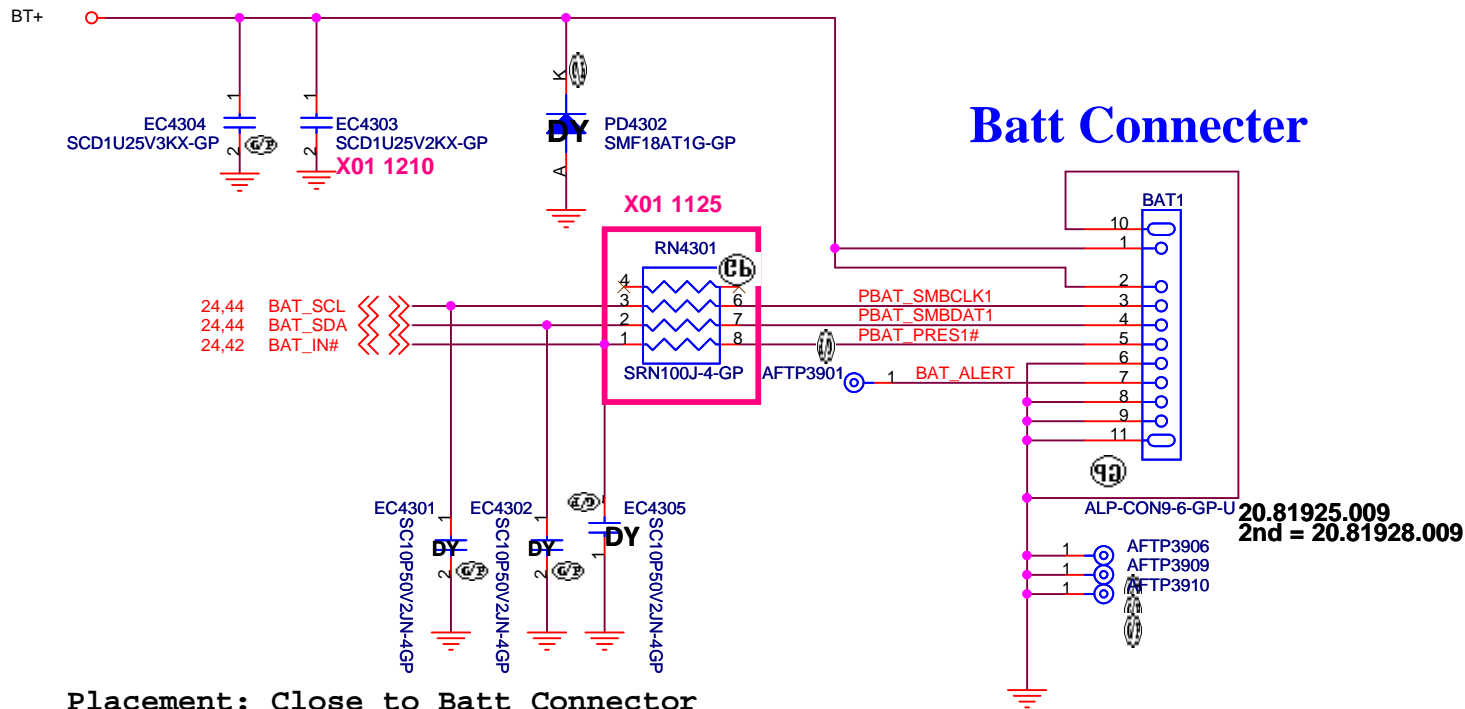
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A4	Document Number Janus AMD BEEMA	Rev A00
Date: Wednesday, March 05, 2014		Sheet 40 of 104

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BEMMA

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Title					
<div>Reserved</div>					
Size	Document Number		Rev		
A4	<div>Janus AMD BEEMA</div>		A00		
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SSID = PWR.Support



75.03101.07D

2nd = 75.00099.E7D

3rd = 75.00099.Q7D

75.03101.07D

2nd = 75.00099.E7D

3rd = 75.00099.Q7D

75.03101.07D

2nd = 75.00099.E7D

3rd = 75.00099.Q7D

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Title

BATT CONN

Size
A4

Document Number

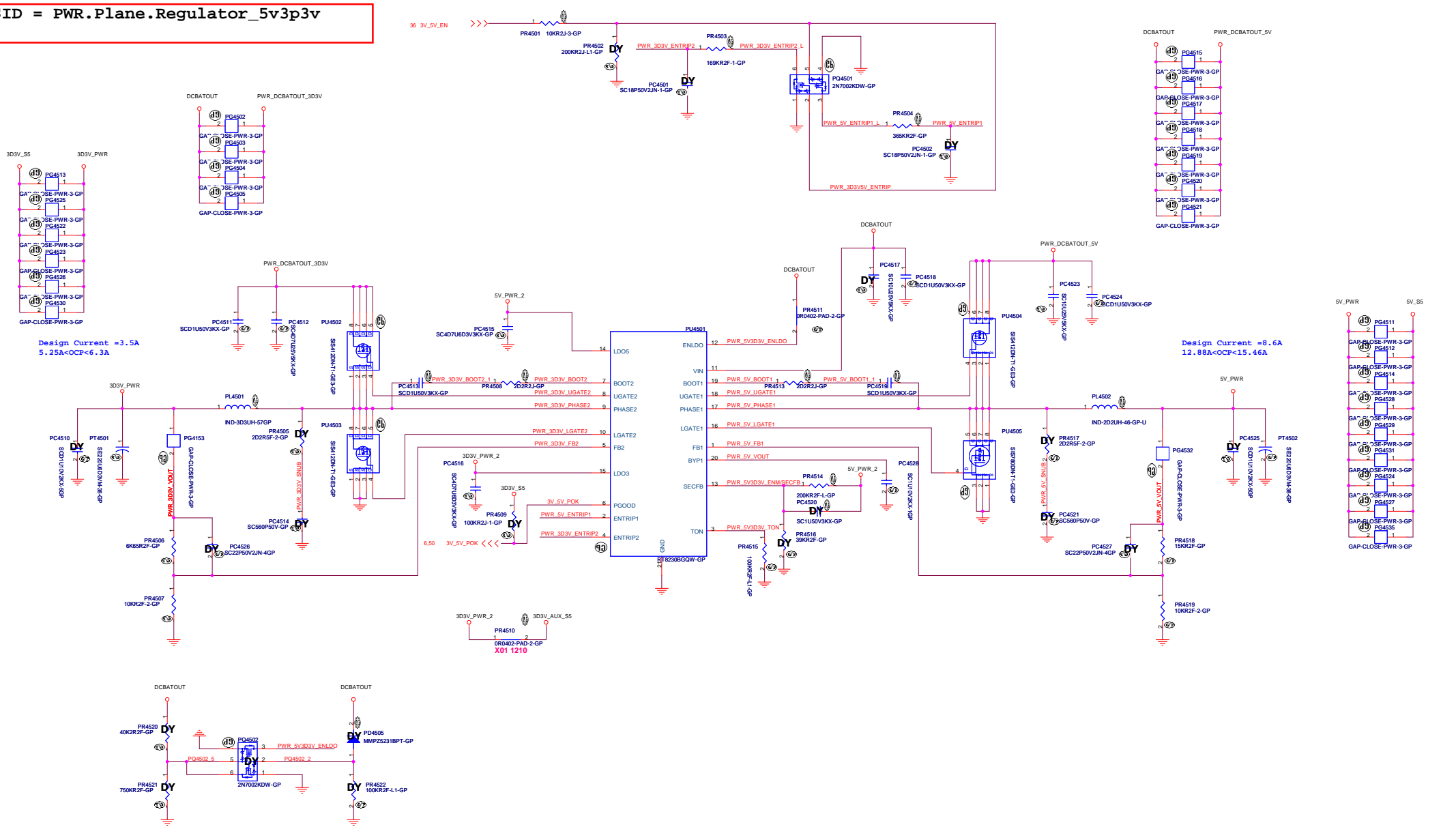
Janus AMD BEEMA

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A00

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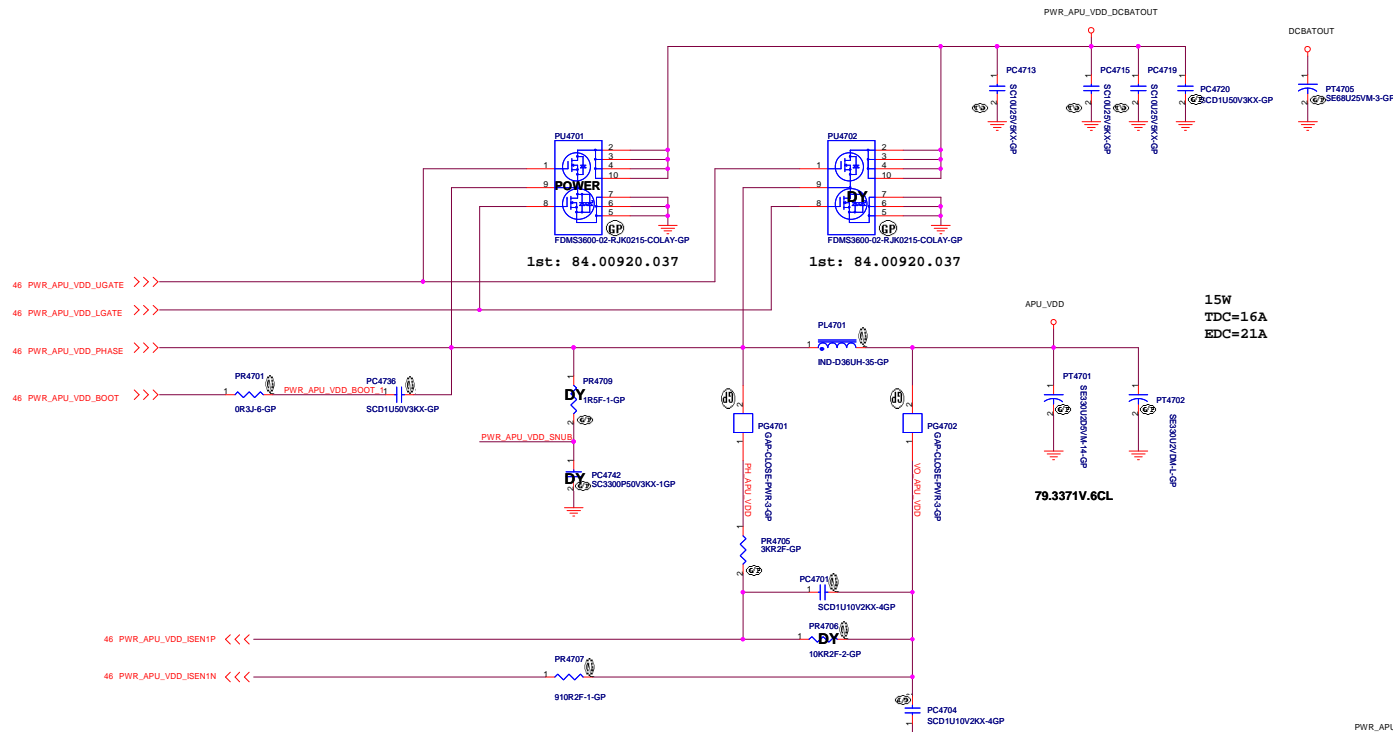
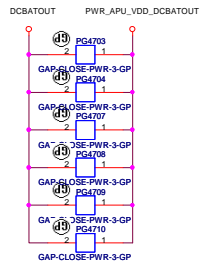
SSID = PWR.Plane.Regulator_5v3p3v



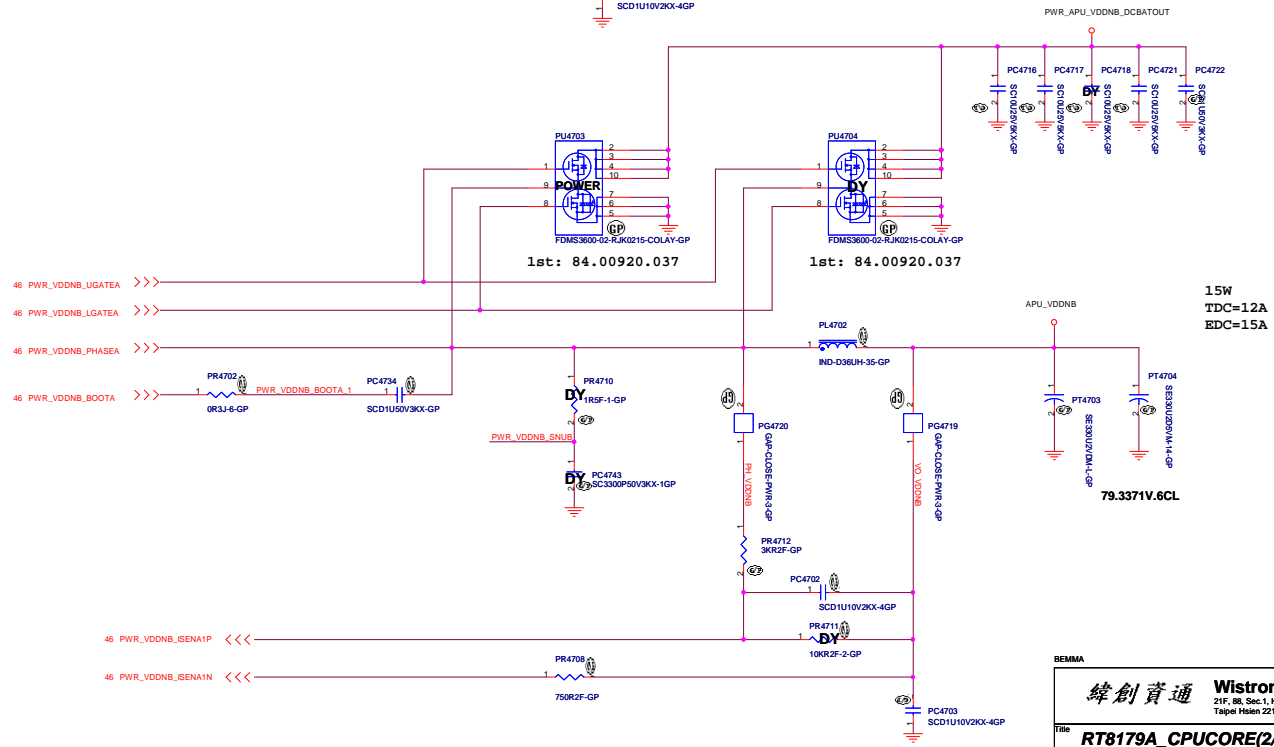
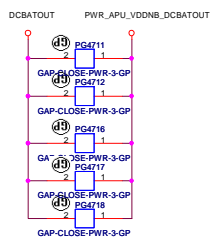
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cynotec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap:CHIP CAP EL 220U 6.3V M6.3*4.4 /Cheml-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOK 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP EL 220U 6.3V M6.3*4.4 /Cheml-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

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15W
TDC=16A
EDC=21A

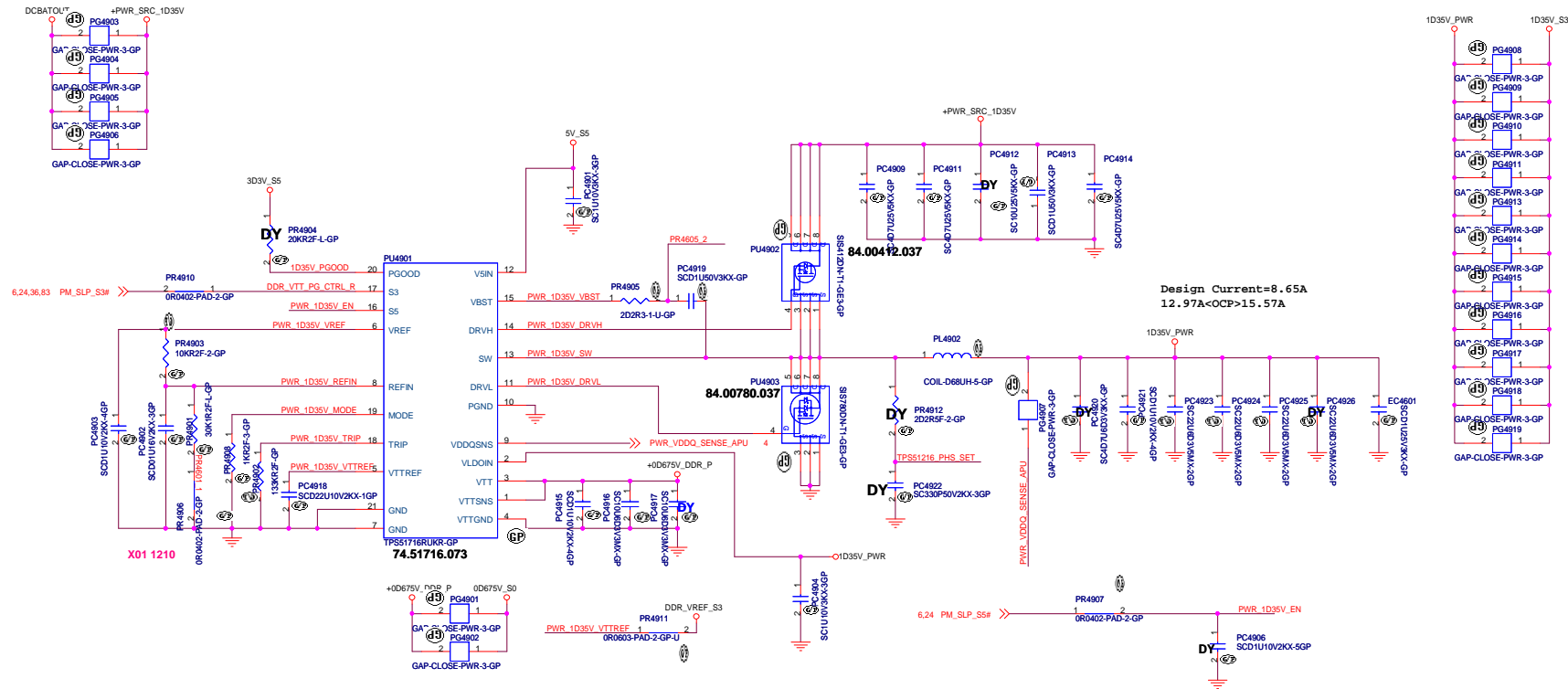


15W
TDC=12A
EDC=15A

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 0.36UH PCME064T-R36MS1R407 1.4mohm / Isat =24Arms 68.R3610.20W
O/P cap:CHIP CAP 470UF 2V EEF5X0D471X /Panasonic/ 6mOhm / 79.47719.2BL
Dual N FET MOS SI2920DT-T1-GE3 DUAL NC POWER 8P /H/S 7.4mohm/8.9mohm / L/S 2.9mOhm/3.5mohm@4.5Vgs / 84.00920.037

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SSID = PWR.Plane.Regulator 1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

TPS51716 MODE

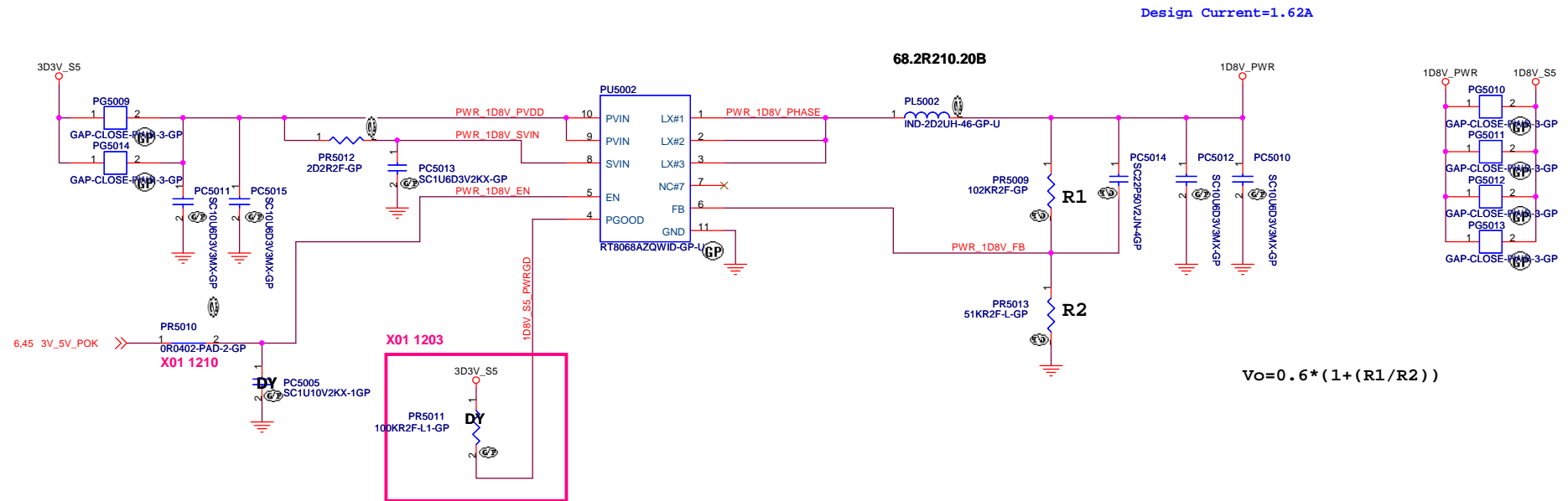
PR4608	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	
1k ohm	500kHz	Tracking Discharge

I/P cap: 10U 25V K0805 X5R / 78.10622.51L
 Inductor: CHIP IND 0.1UH M PCMC063T-R10MN 1.5-1.7mohm Isat =60Arms 68.R1010.10T
 O/P cap: CHIP CAP C 22U 6.3V M0805 X5R / 78.22610.51L
 H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
 L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

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SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S5



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Title			RT8068A 1D8V_S5
Size	Document Number	Rev	A00
A3	Janus AMD BEEMA		
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SSID = PWR.Plane.Regulator_1p5v

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Title		Rev	
TLV70215_1D5		A00	
Size	Document Number	Date: Wednesday, March 05, 2014	
A3	Janus AMD BEEMA	Sheet	51 of 104

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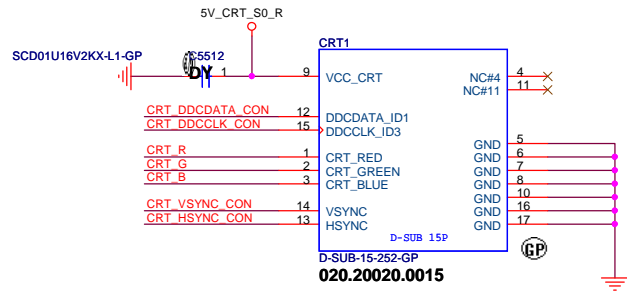
BEMMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
(Reserved)			
Size	Document Number	Rev	
A3	Janus AMD BEEMA	A00	
Date: Wednesday, March 05, 2014		Sheet	53 of 104

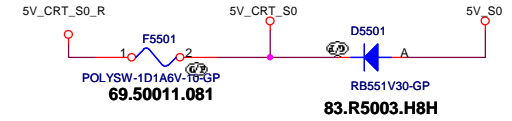
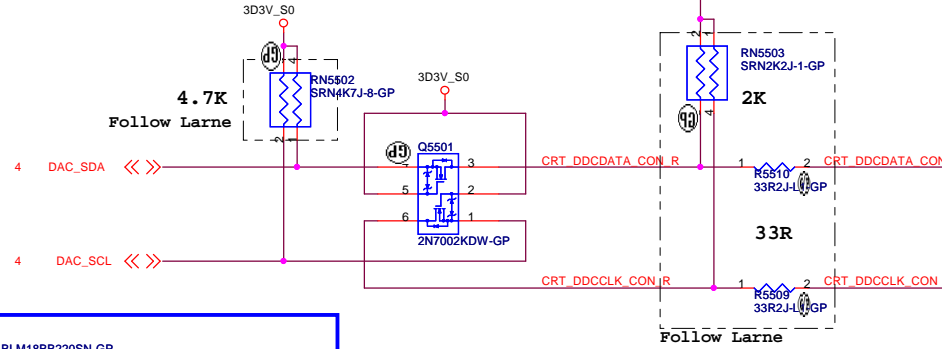
SSID = VIDEO

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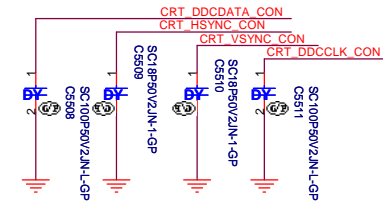
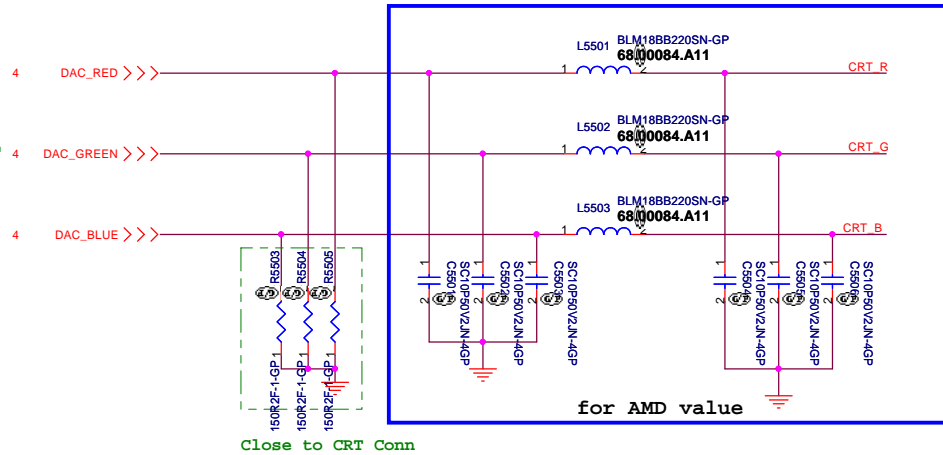
CRT Board Connector



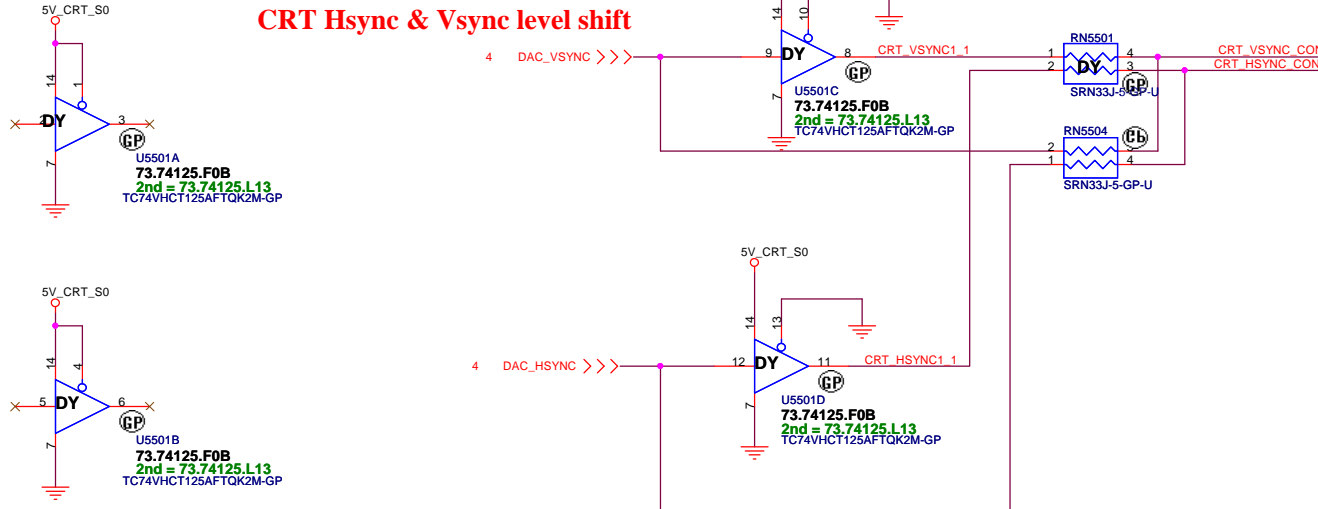
CRT DDCDATA & DDCCLK level shift



APU to CRT



CRT Hsync & Vsync level shift



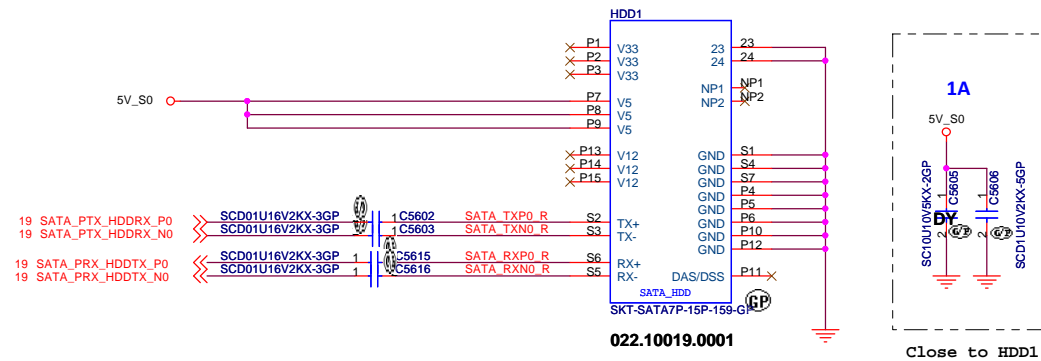
<http://sualaptop365.edu.vn>

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VGA Con.	
Size A3	Document Number
Janus AMD BEEMA	
Date: Wednesday, March 05, 2014	Sheet 55 of 104

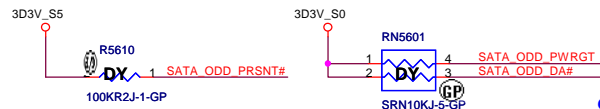
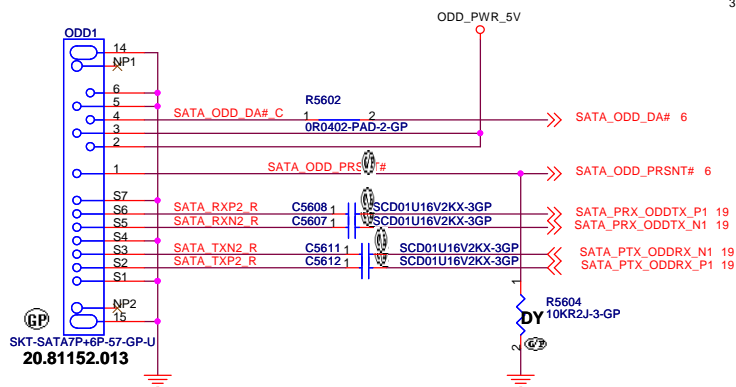
SSID = SATA

SATA HDD Connector

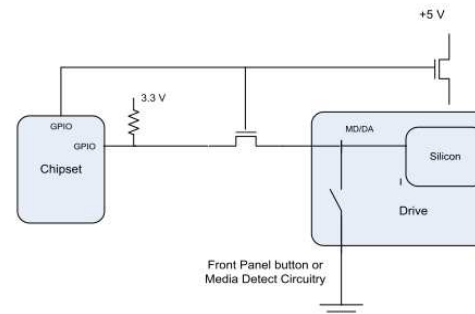
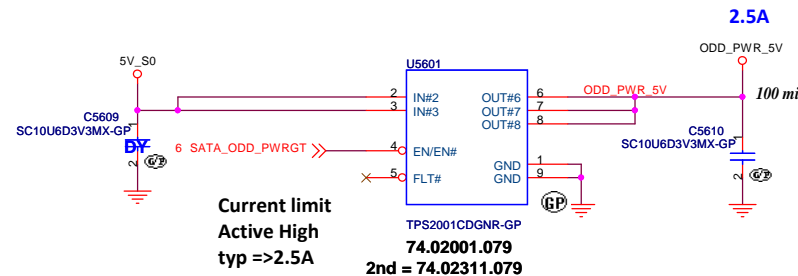


ME Note: New HDD conn symbol is not ready,
we will use original OAK HDD conn (22.10300.991) and shift to the correct position.

ODD Connector



SATA Zero Power ODD



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Title

HDD/ODD

Size
A3

Document Number

Janus AMD BEEMA

Rev
A00

Date: Wednesday, March 05, 2014

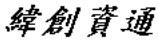
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SSID = ESATA

(Blanking)

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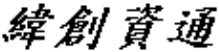
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ESATA			
Size A3	Document Number Janus AMD BEEMA		Rev A00
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Title			
Reserved			
Size A4	Document Number Janus AMD BEEMA		Rev A00
Date: Wednesday, March 05, 2014	Sheet	59	of 104

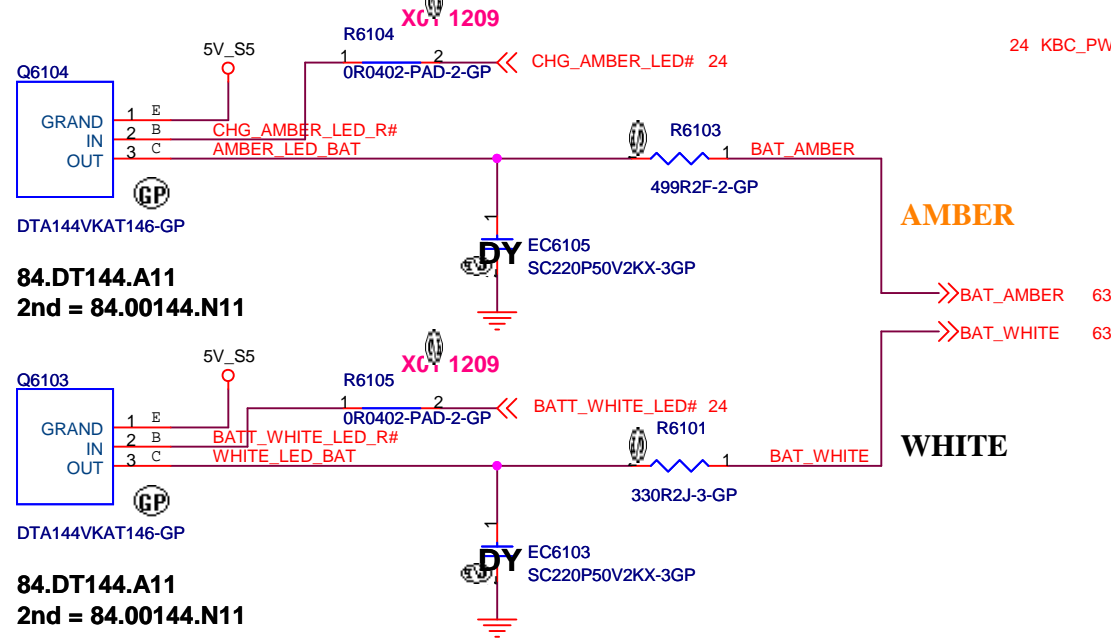
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BEMMA			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Janus AMD BEEMA		Rev A00
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SSID = User.Interface

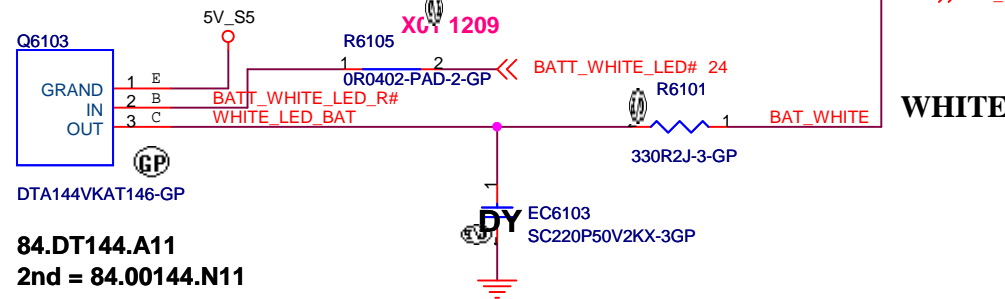
Battery LED1 (AMBER_LED)

Low activated from KBC GPIO

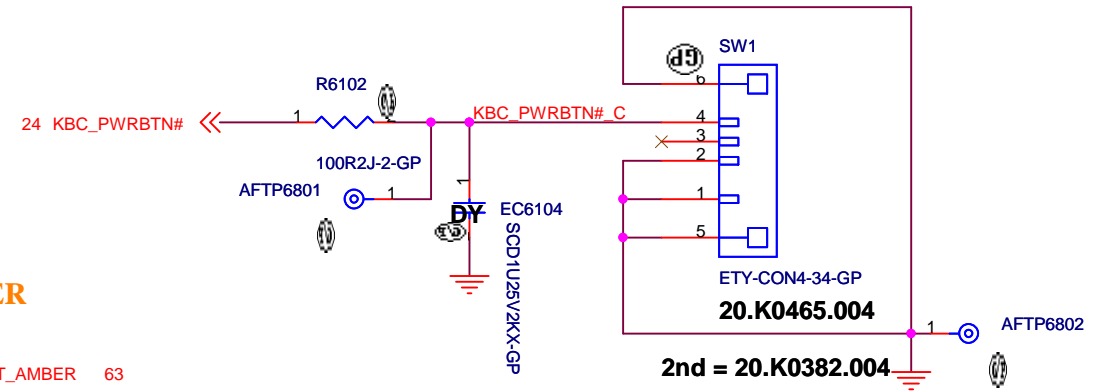


Battery LED2 (WHITE_LED)

Low activated from KBC GPIO



Power button



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Title

LED Bard/Power Button

Size
A4

Document Number

Janus AMD BEEMA

Rev

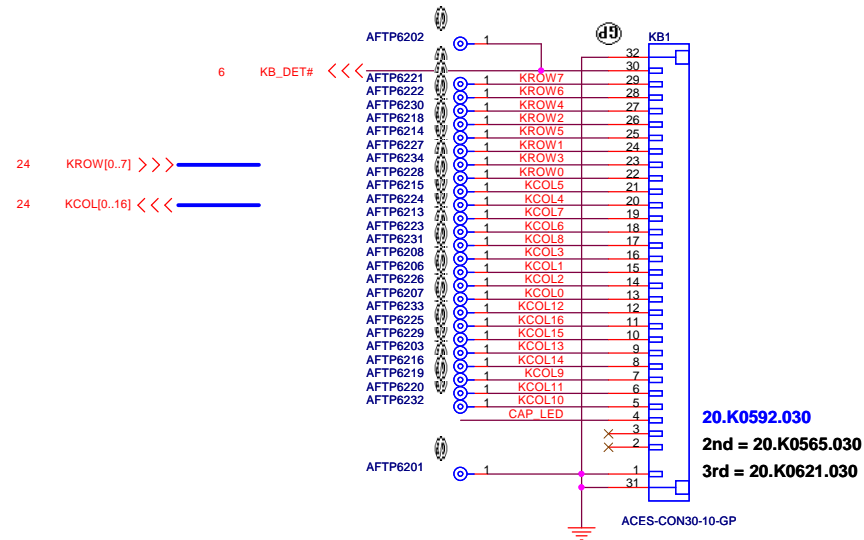
A00

Date: Wednesday, March 05, 2014

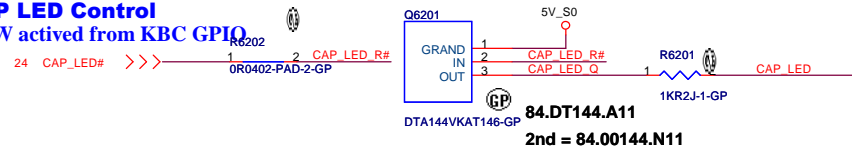
Sheet 61 of 104

SSID = KBC

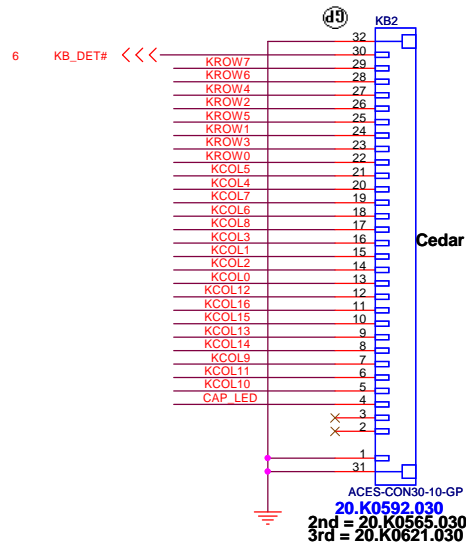
Internal Keyboard Connector (DVC40)



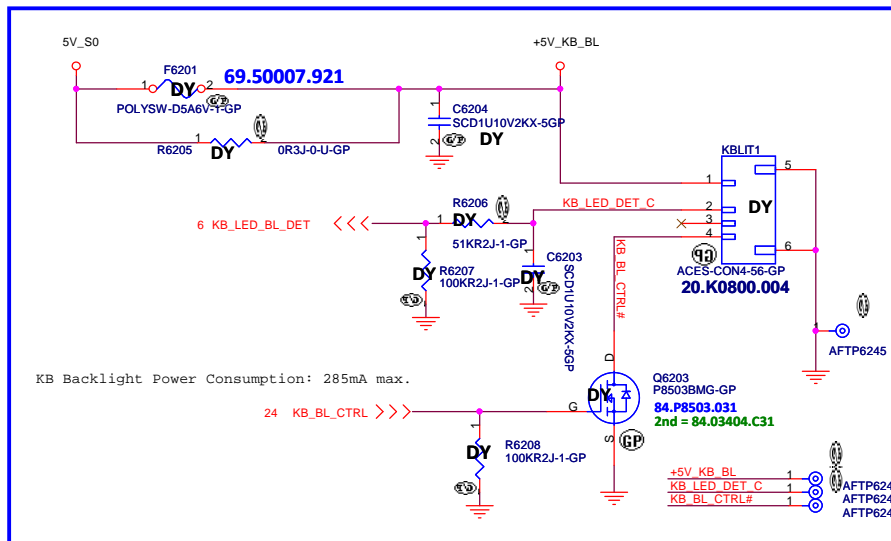
CAP LED Control
LOW actived from KBC GPIO



Internal Keyboard Connector (DVC50)



Keyboard Backlight (DVC50)

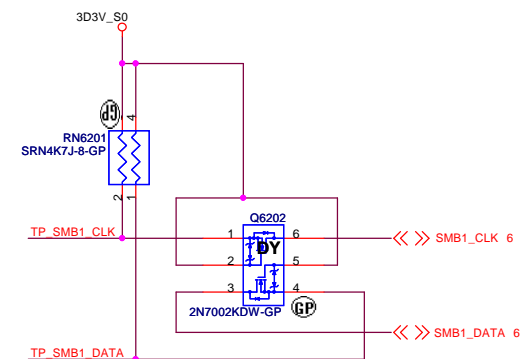
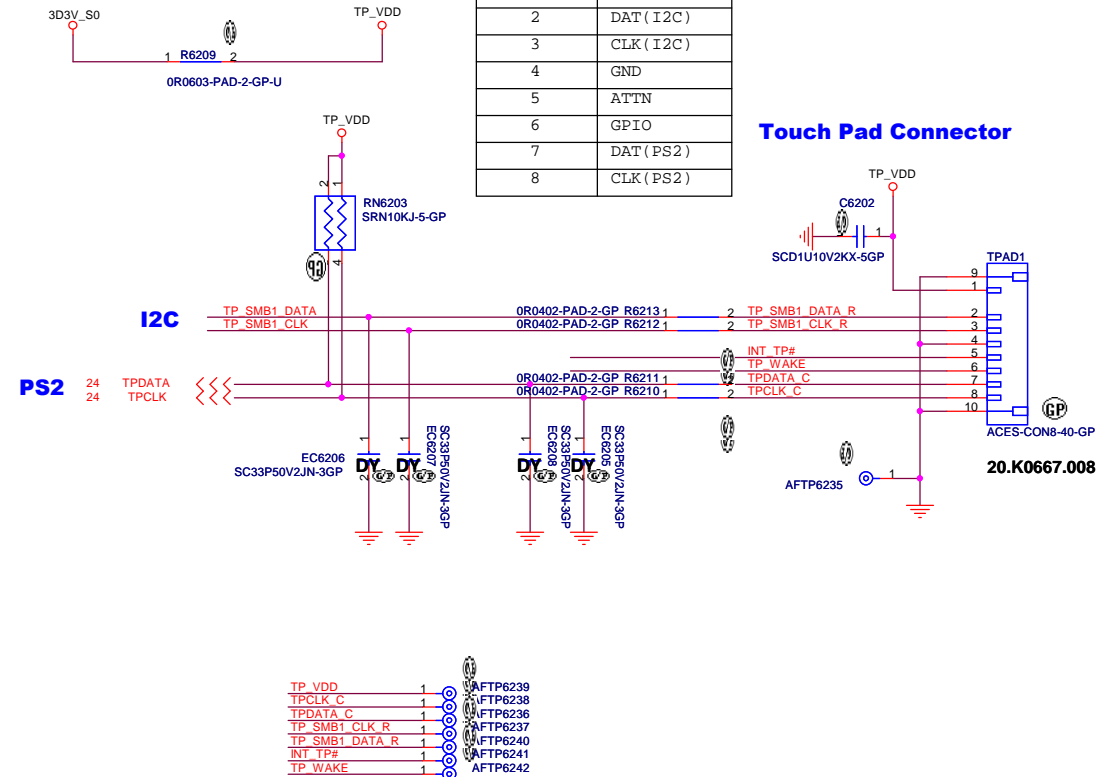


KB Backlight Power Consumption: 285mA max.

```
SSID = Touch.Pad
```

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

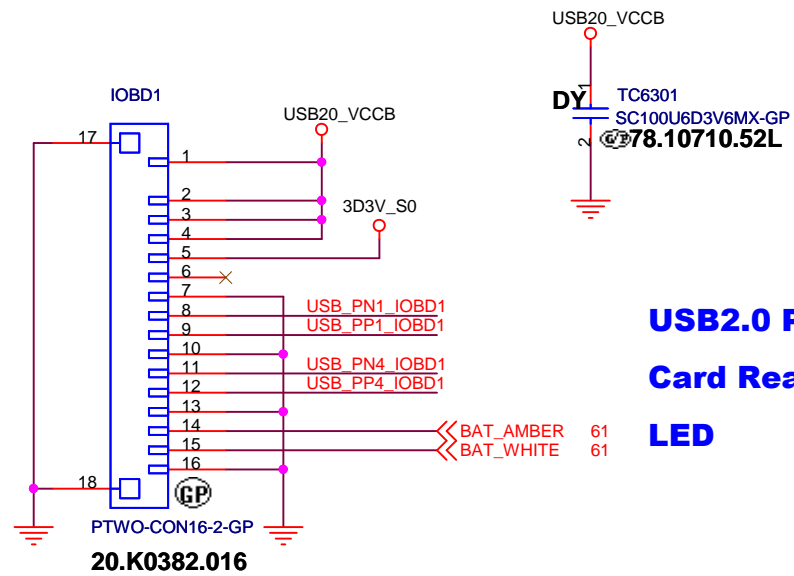
Touch Pad Connector



BEMMA

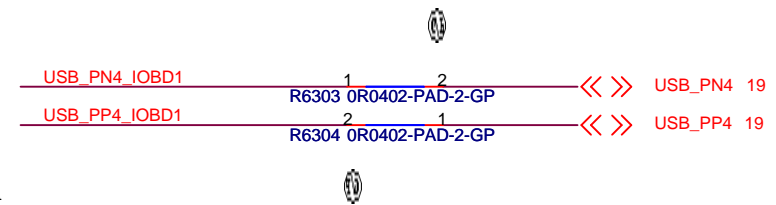
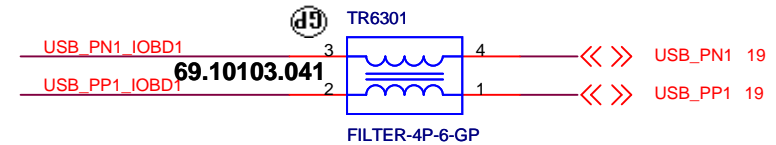
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
Key Board/Touch Pad			
Size A3	Document Number		Rev
	Janus AMD BEEMA		A00
Date:	Wednesday, March 05, 2014	Sheet 62 of 104	



USB2.0 Port3 Card Reader LED

The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA



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Title

IO Board Connector

Size
A4

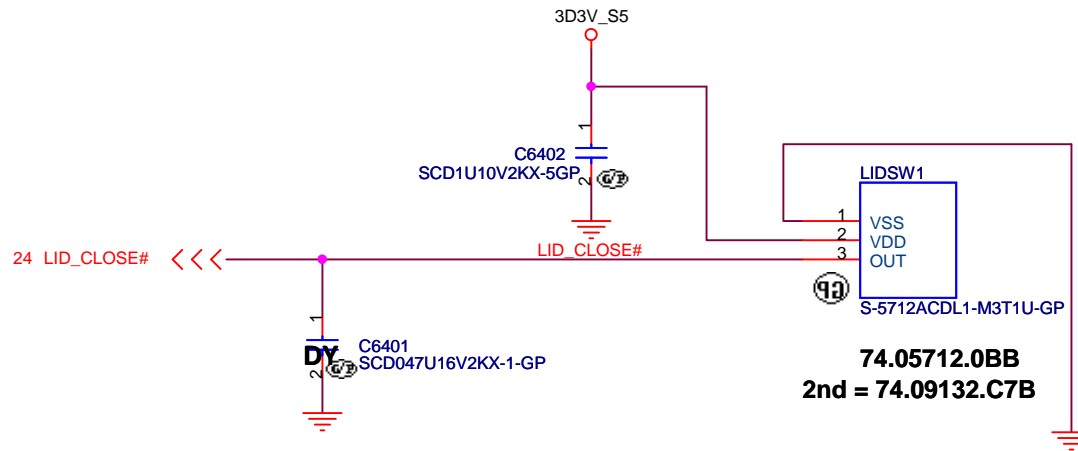
Document Number
Janus AMD BEEMA

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A00

Date: Wednesday, March 05, 2014

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SSID = User.Interface



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Title

Hall Sensor

Size
A4

Document Number

Janus AMD BEEMA

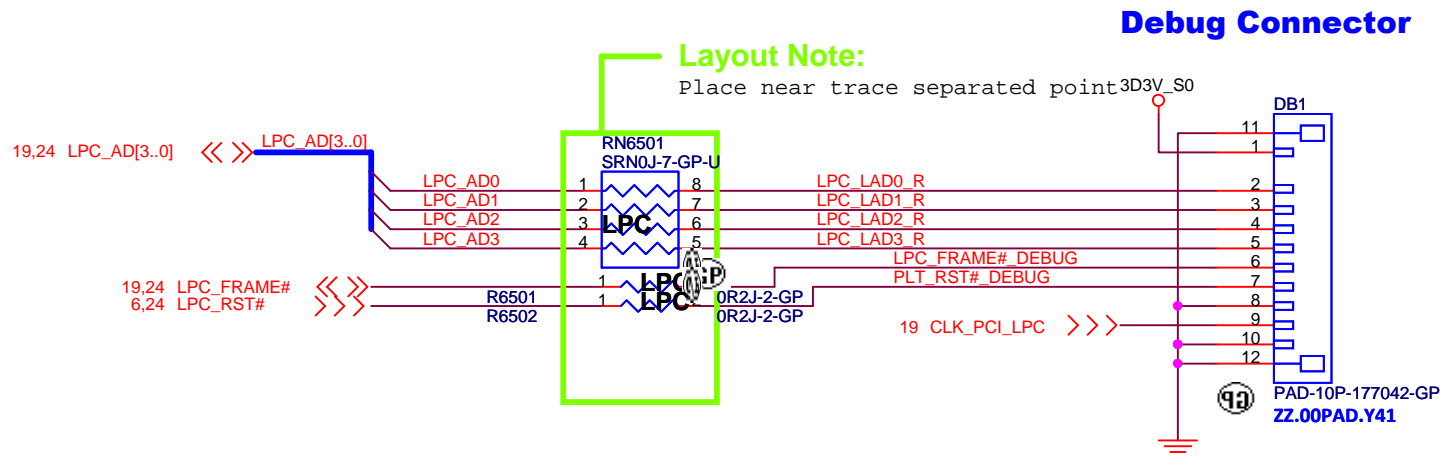
Rev
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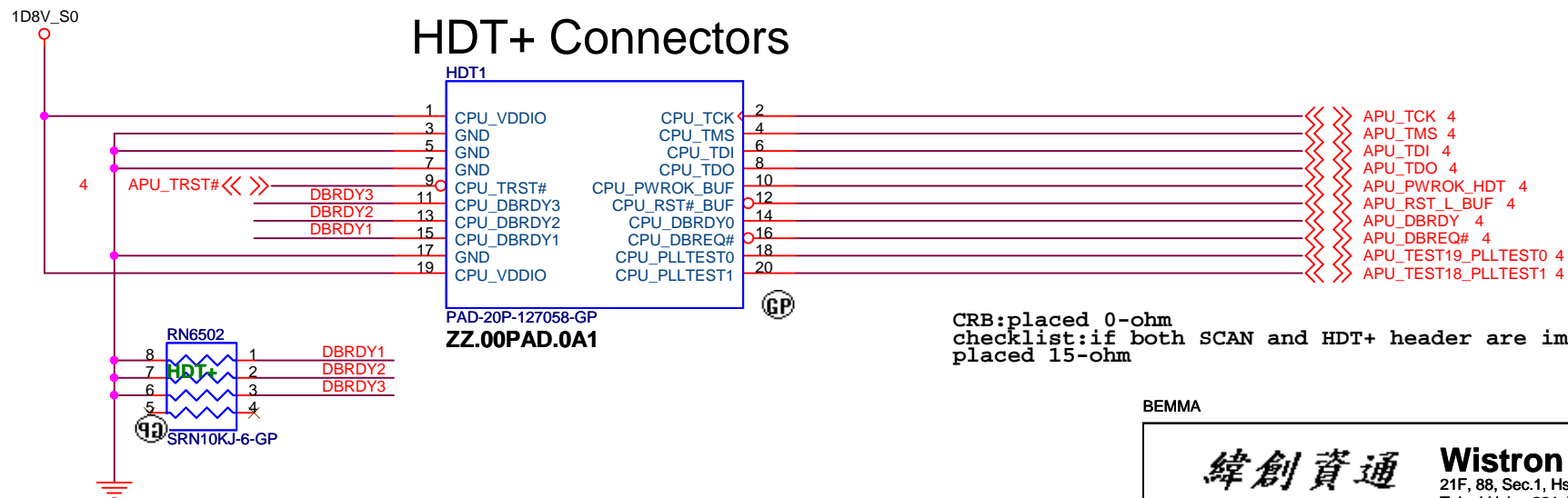
<http://sualaptop365.edu.vn>

SSID = DEBUG PORT



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

HDT+ Connectors



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Title

Dubug connector

Size
A4

Document Number

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		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
<div>Title</div>					
<div>Reserved</div>					
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>		
<div>A4</div>	<div>Janus AMD BEEMA</div>		<div>A00</div>		
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reserved			
Size	Document Number	Rev	
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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (1/5)

Size
A4

Document Number

Janus AMD BEEMA

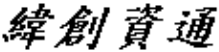
Rev
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Title Thunderbolt (2/5)			
Size A4	Document Number Janus AMD BEEMA		Rev A00
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Size A4	Document Number Janus AMD BEEMA	Rev A00
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (4/5)

Size
A4

Document Number

Janus AMD BEEMA

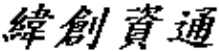
Rev
A00

Date: Wednesday, March 05, 2014

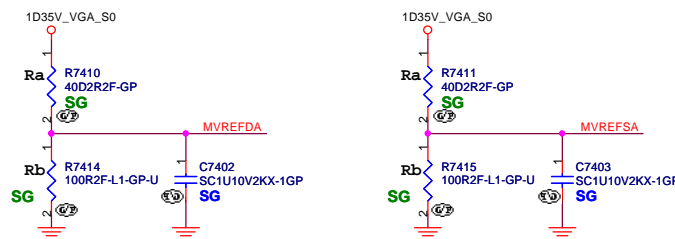
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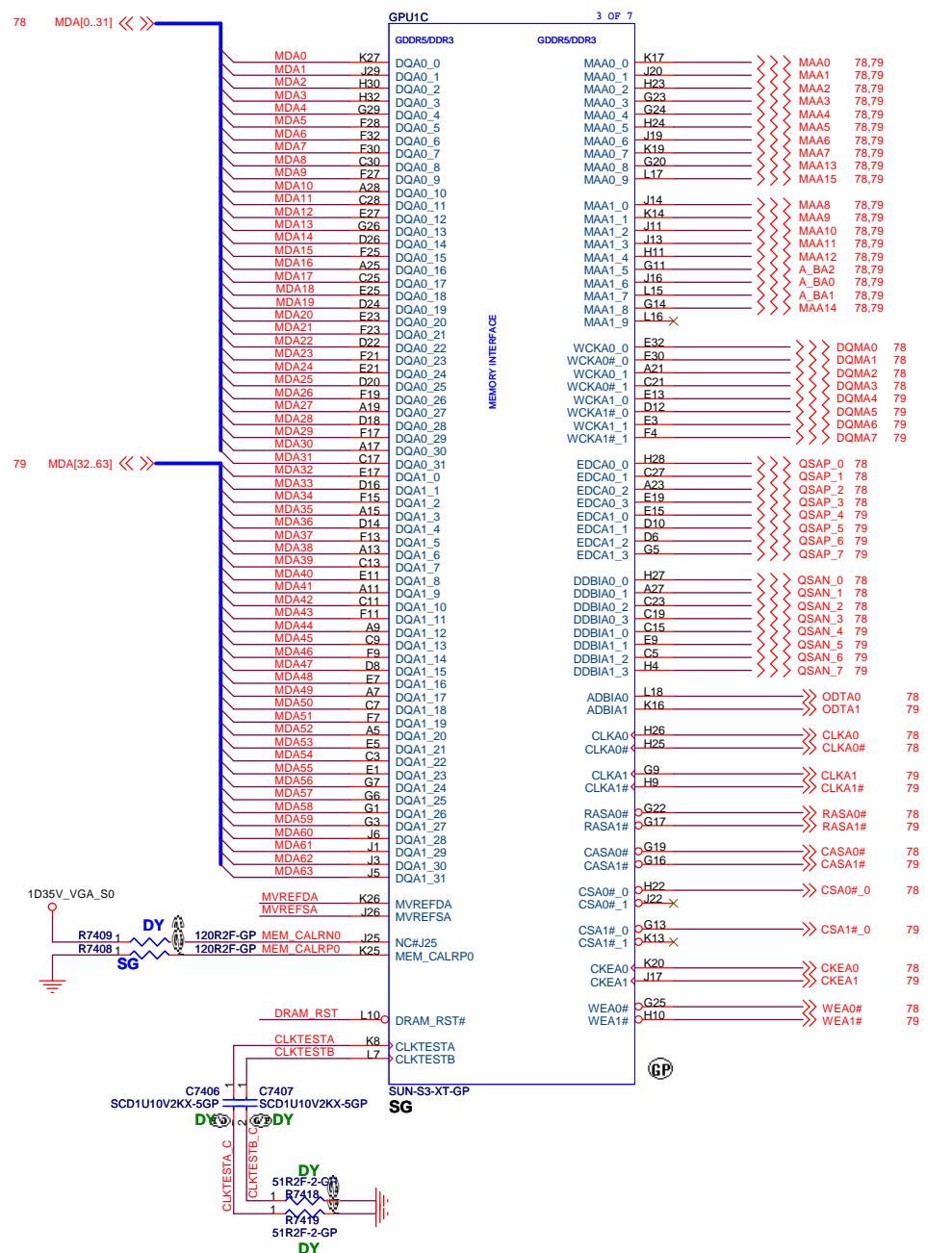
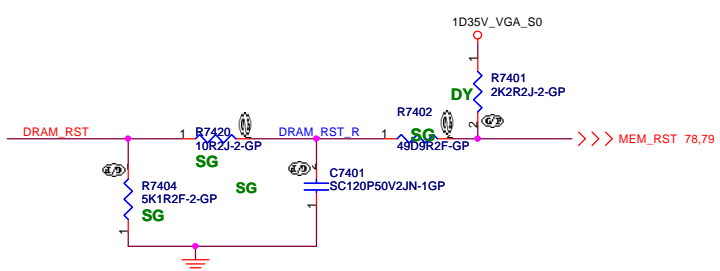
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Size A4	Document Number Janus AMD BEEMA		Rev A00
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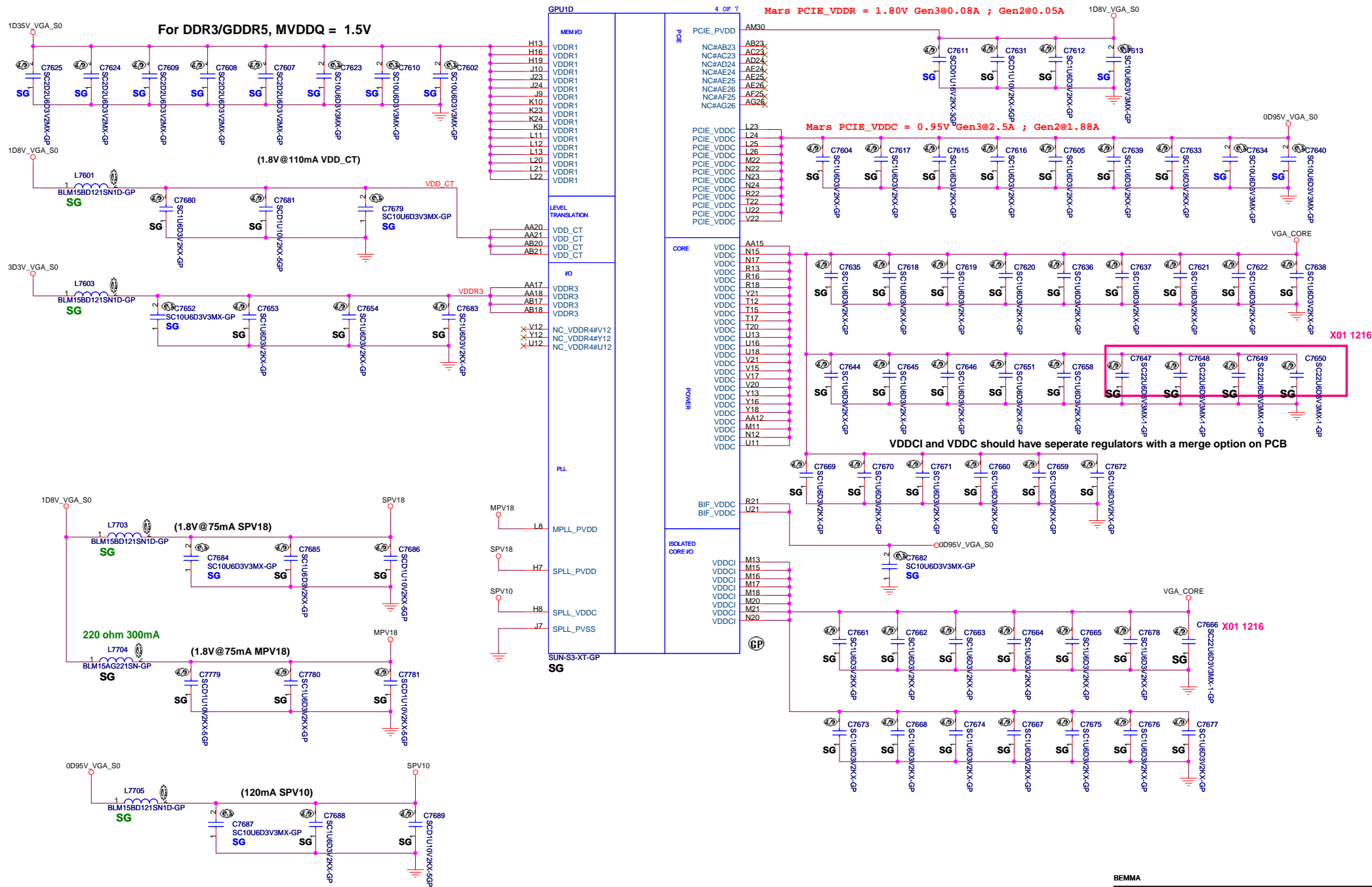
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.35V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R





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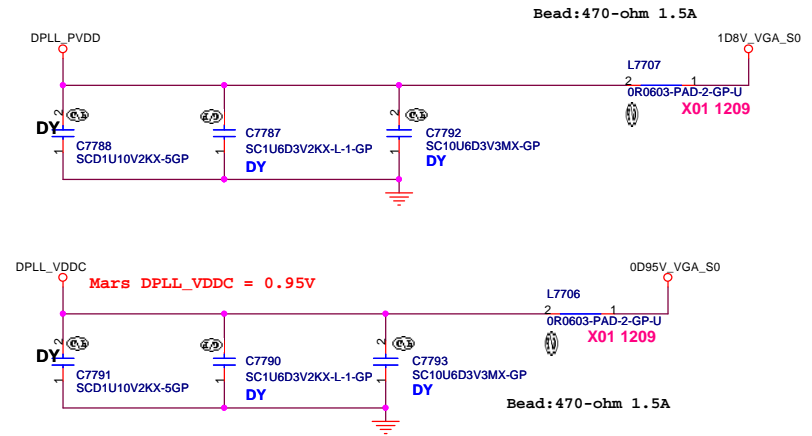
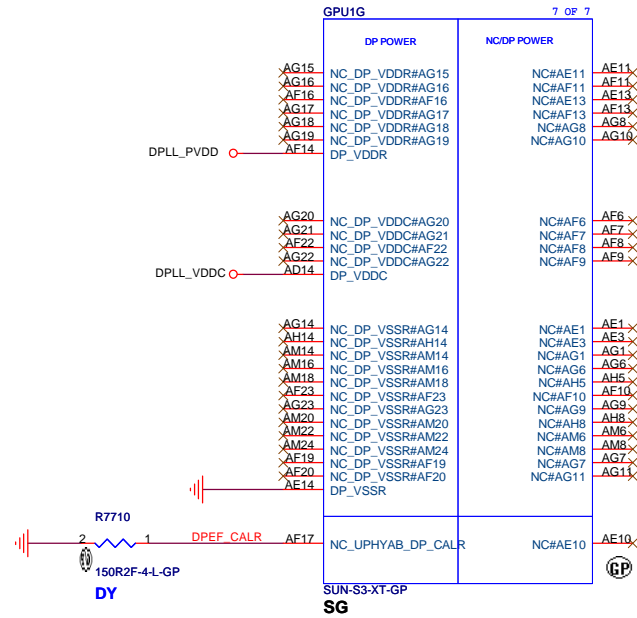
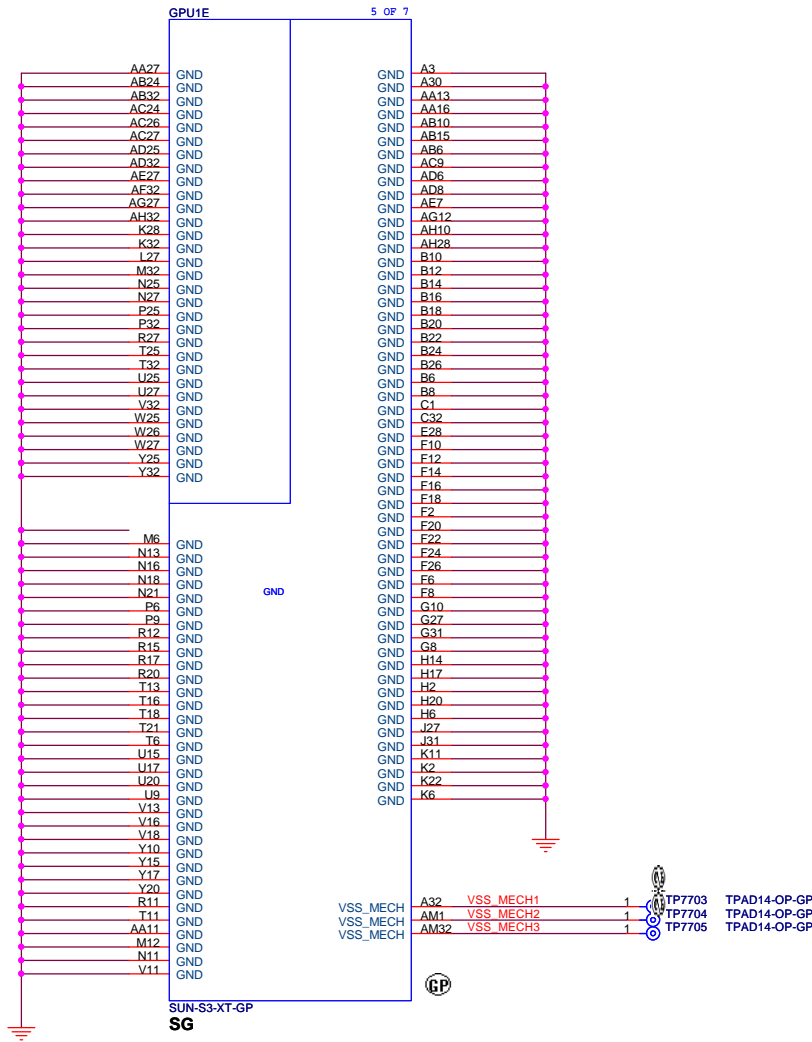
緯創資通

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Title **GPU_GPIO/STRAP**

Size Document Number **Janus AMD BEEMA** Rev **A00**

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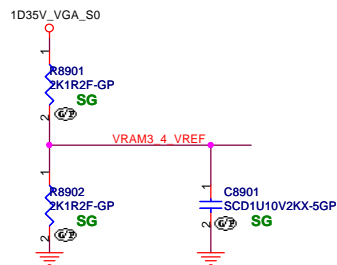
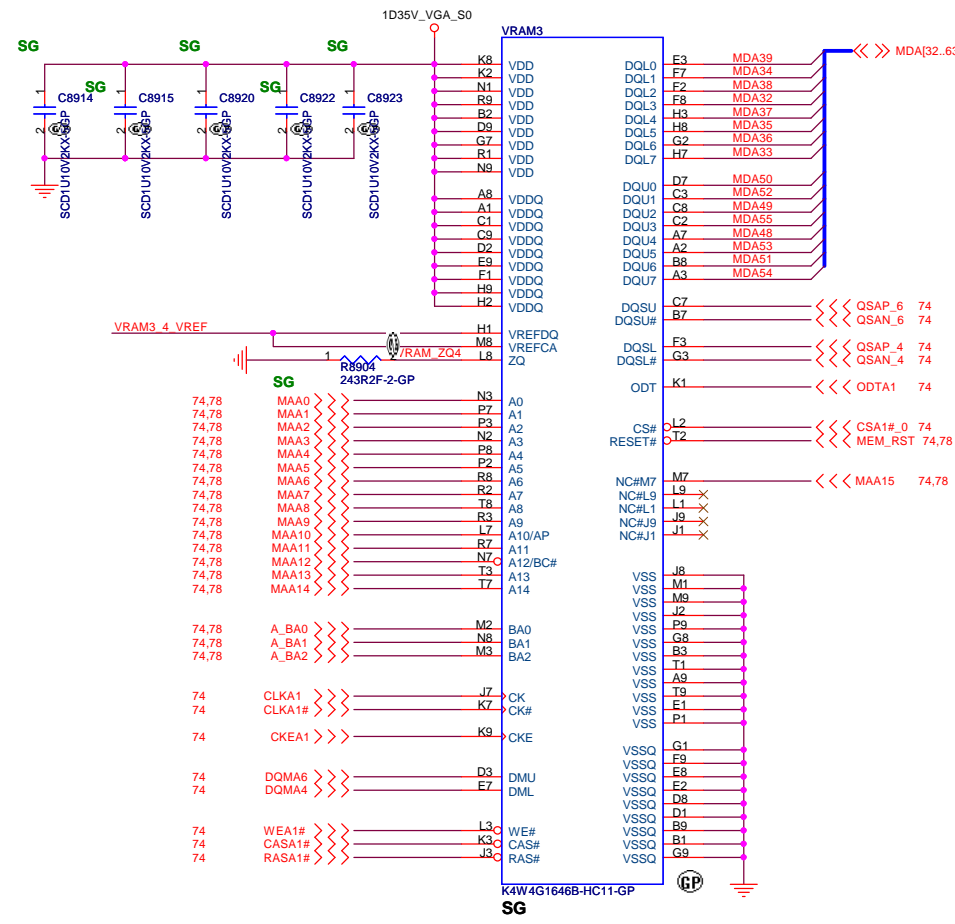
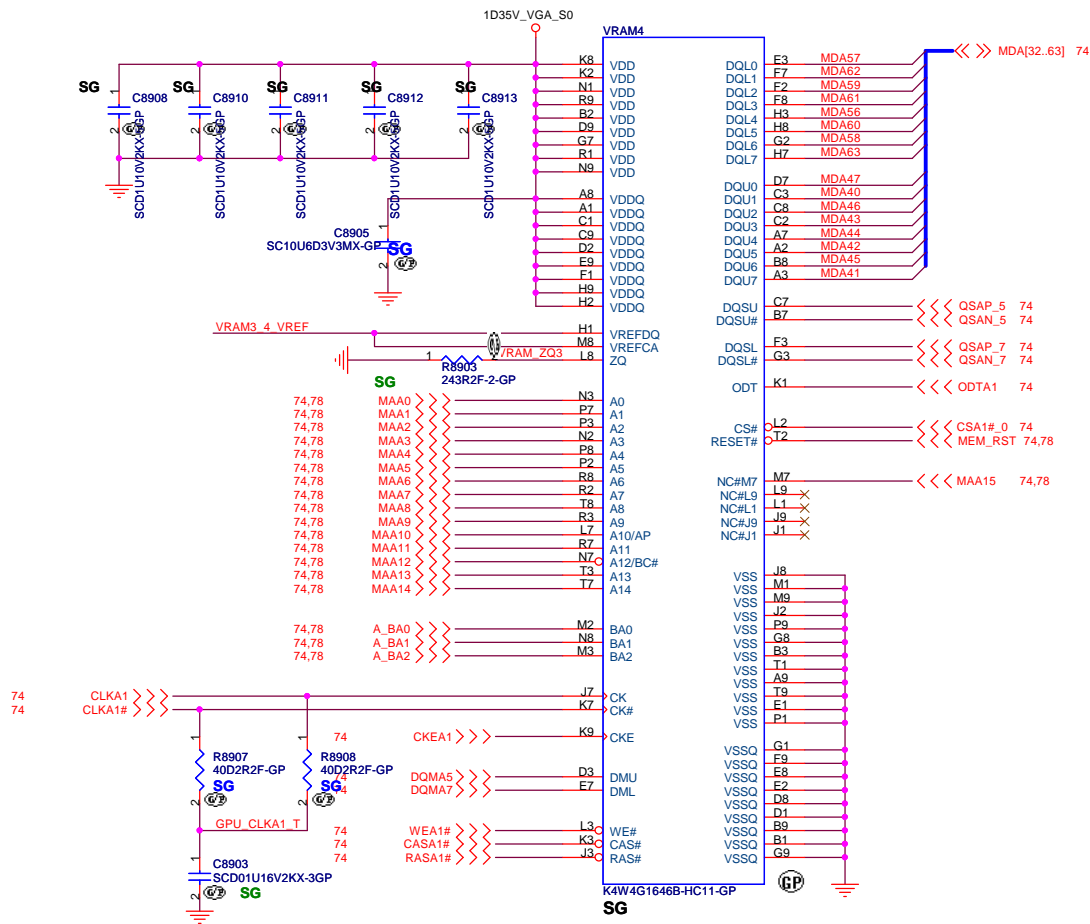
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Taipei Hsien 221, Taiwan, R.O.C.

Title GPU_POWER/GND
Size Project Name
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緯創資通 Wistron Corporation
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Title			
GPU-VRAM1,2 (1/4)			
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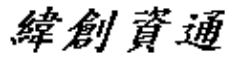
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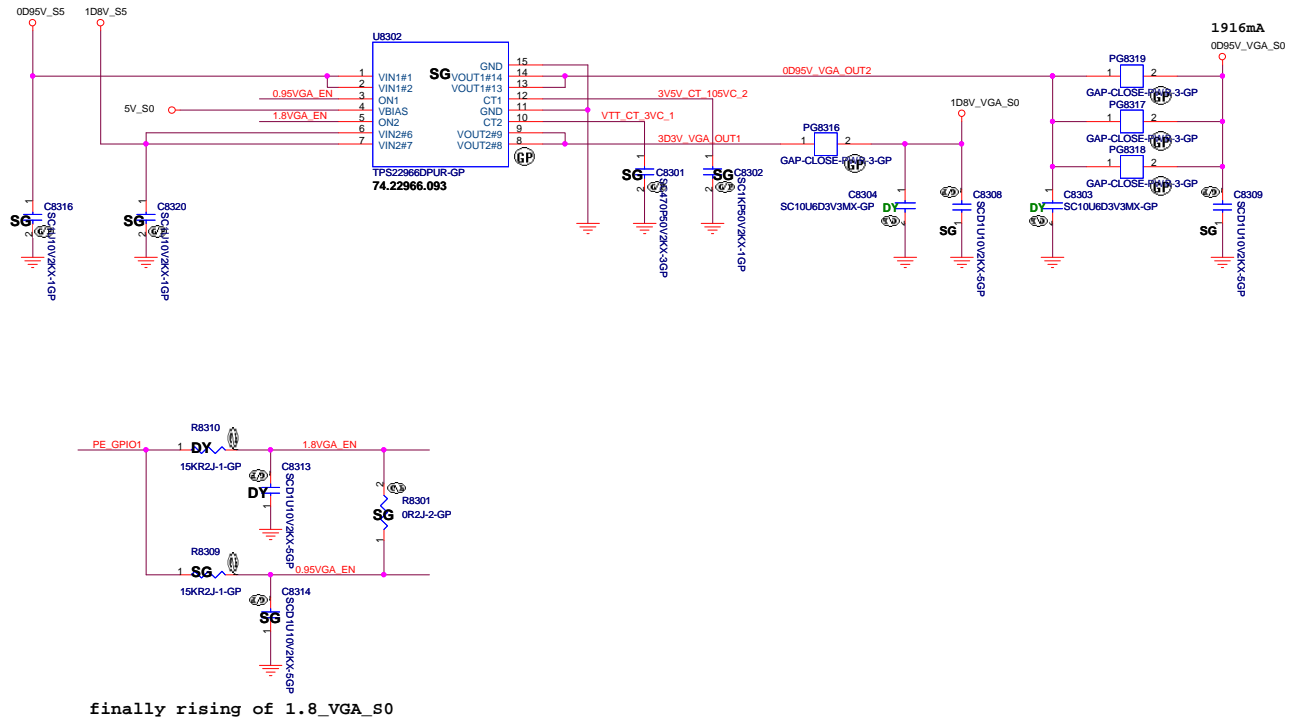
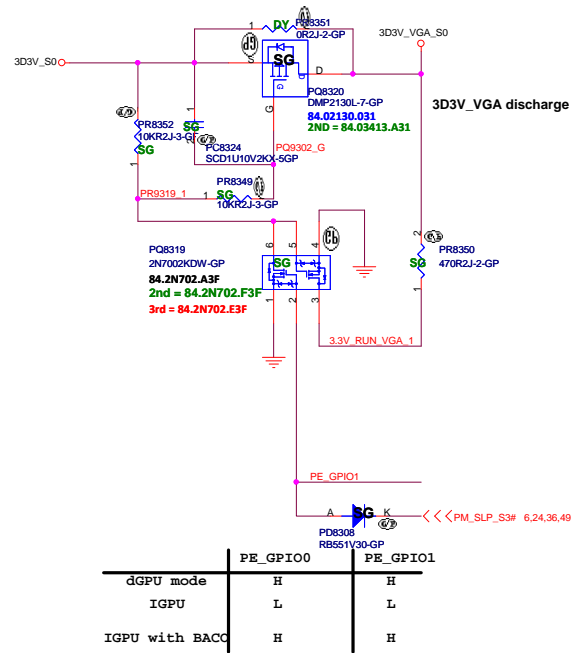
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Size A4	Document Number Janus AMD BEEMA		Rev A00
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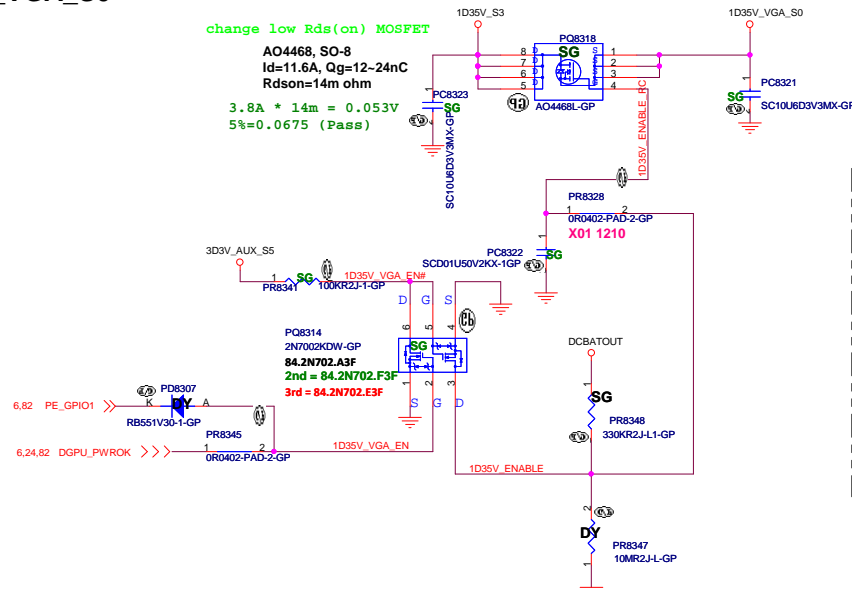
3D3V_S0 to 3D3V_VGA_S0 Transfer

Change DUMMY Reference Name to PX_BACO

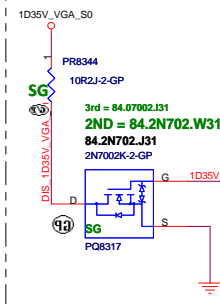


1D5V_VGA_S0

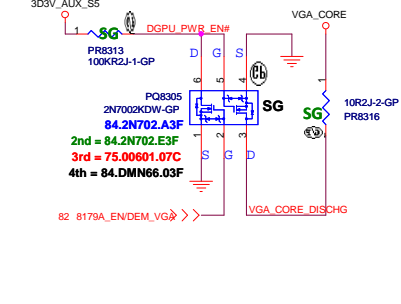
change low $R_{ds(on)}$ MOSFET
 AO4468, SO-8
 $I_d=11.6A$, $Q_g=12-24nC$
 $R_{ds(on)}=14m\ ohm$
 $3.8A * 14m = 0.053V$
 $5\% = 0.0675$ (Pass)



Discharge Circuit



VGA_CORE Discharge Circuit



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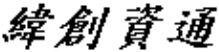
DISCRETE VGA POWER			
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Custom		A00	
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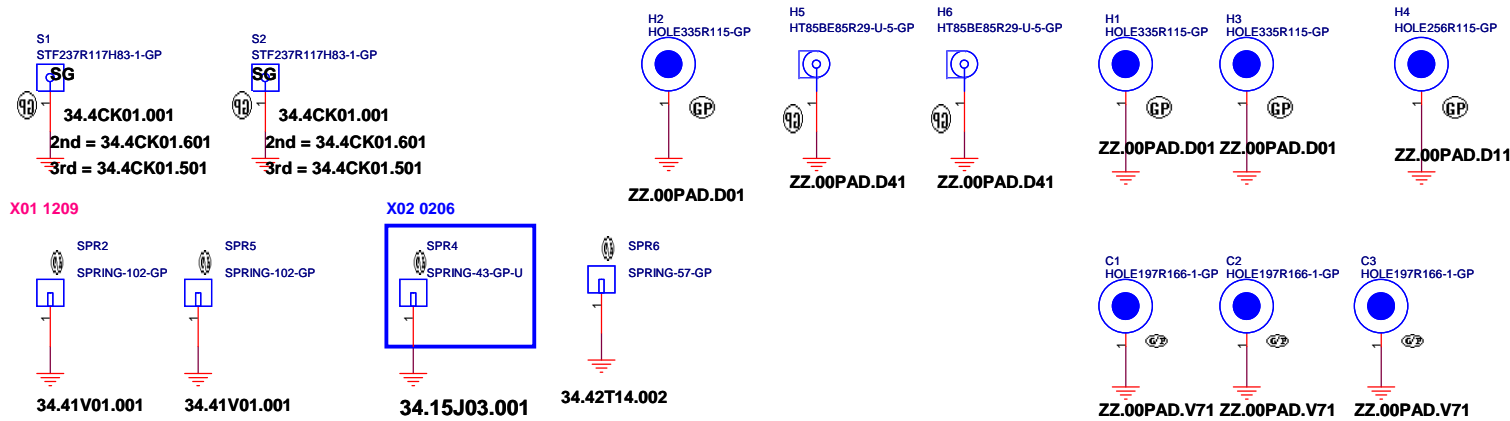
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Title <div>(Reserved)</div>		
Size <div>A4</div>	Document Number <div>Janus AMD BEEMA</div>	Rev <div>A00</div>
Date <div>Wednesday, March 05, 2014</div>		Sheet <div>84</div> of <div>104</div>

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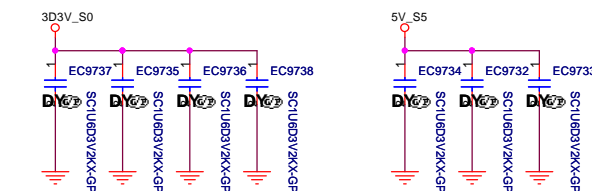
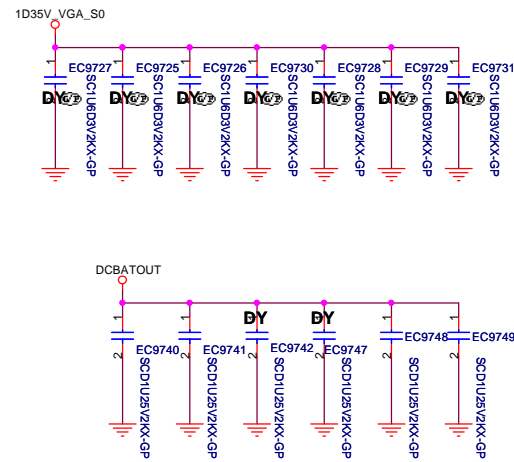
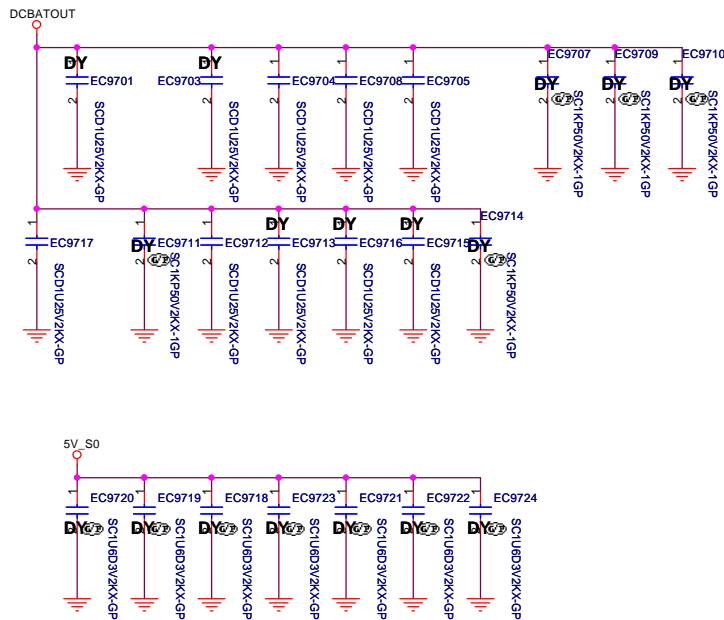
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SSID = Mechanical



SSID = EMI



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Title UNUSED PARTS/EMI Capacitors			
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
NFC(Reserved)		
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Title			
TPM/TCM			
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Title TEST PAD		
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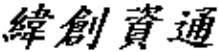
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Title (Reserved)			
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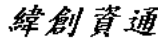
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Title			
MCP CPU XDP HDT+			
Size A3	Document Number		Rev
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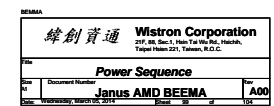
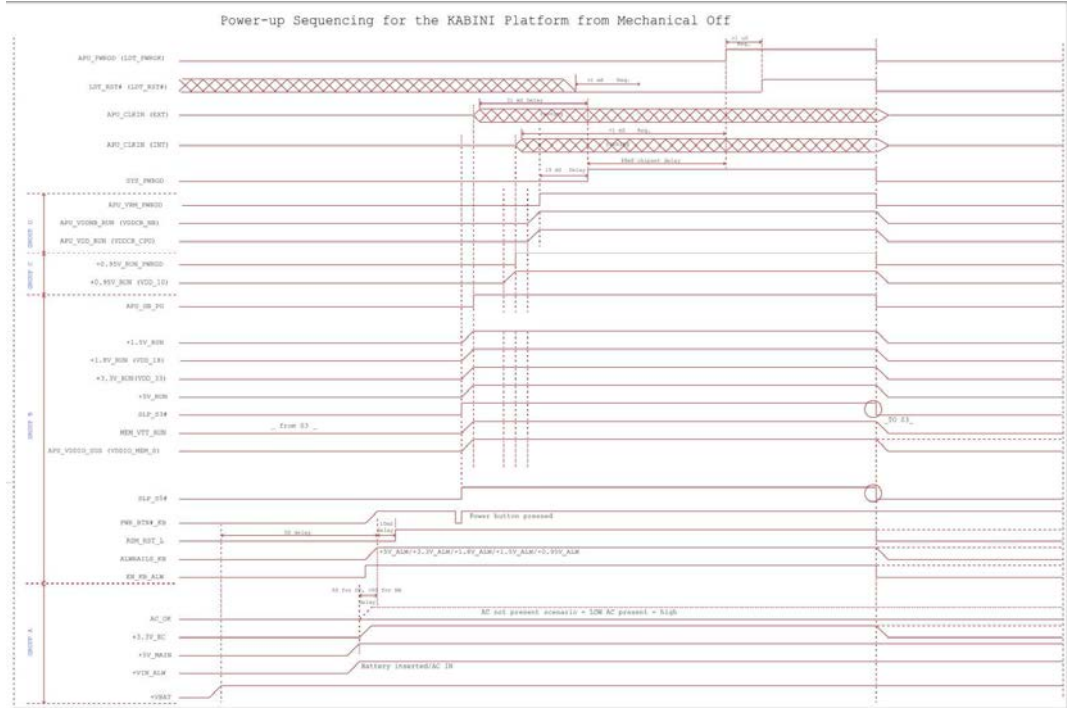
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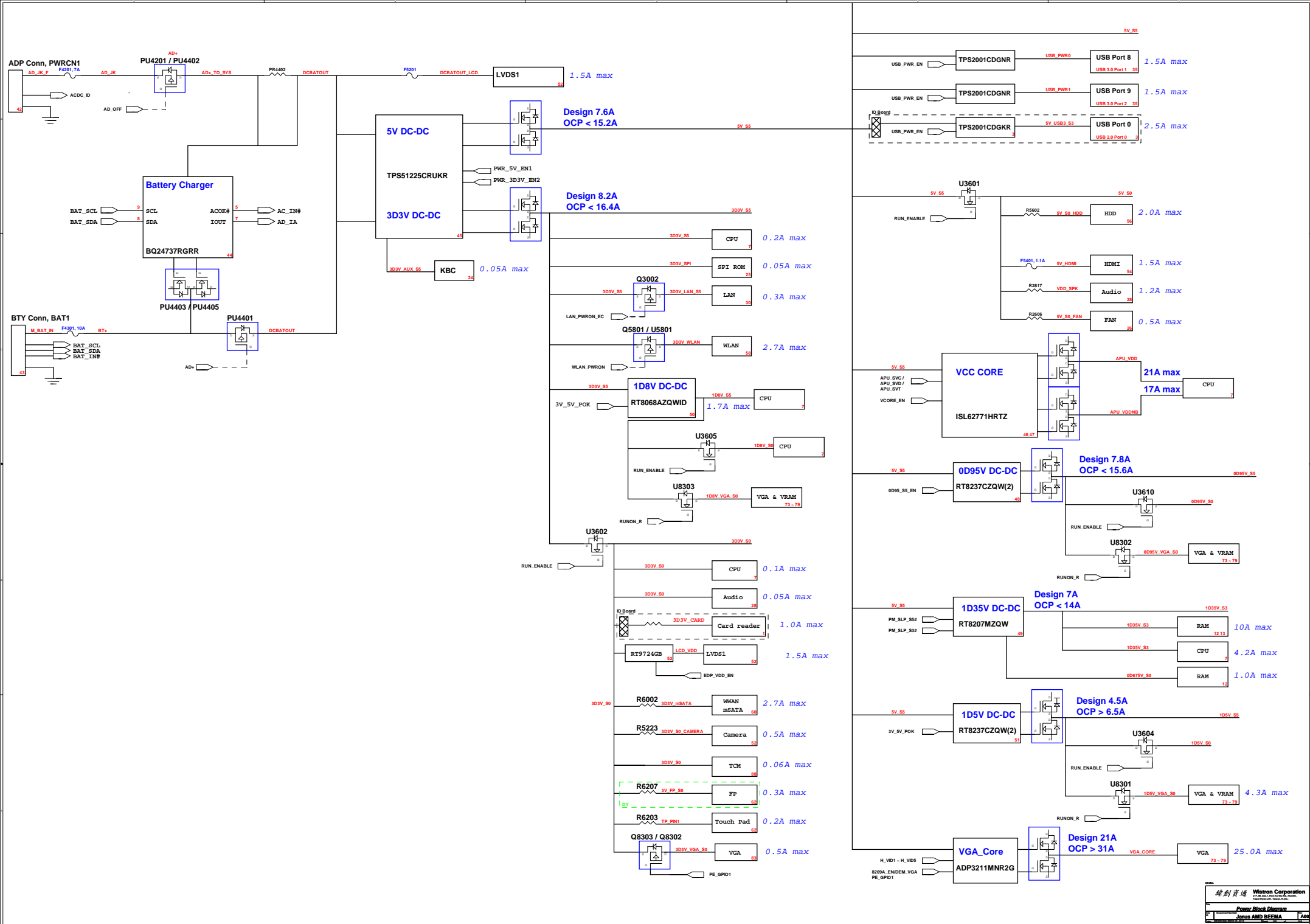
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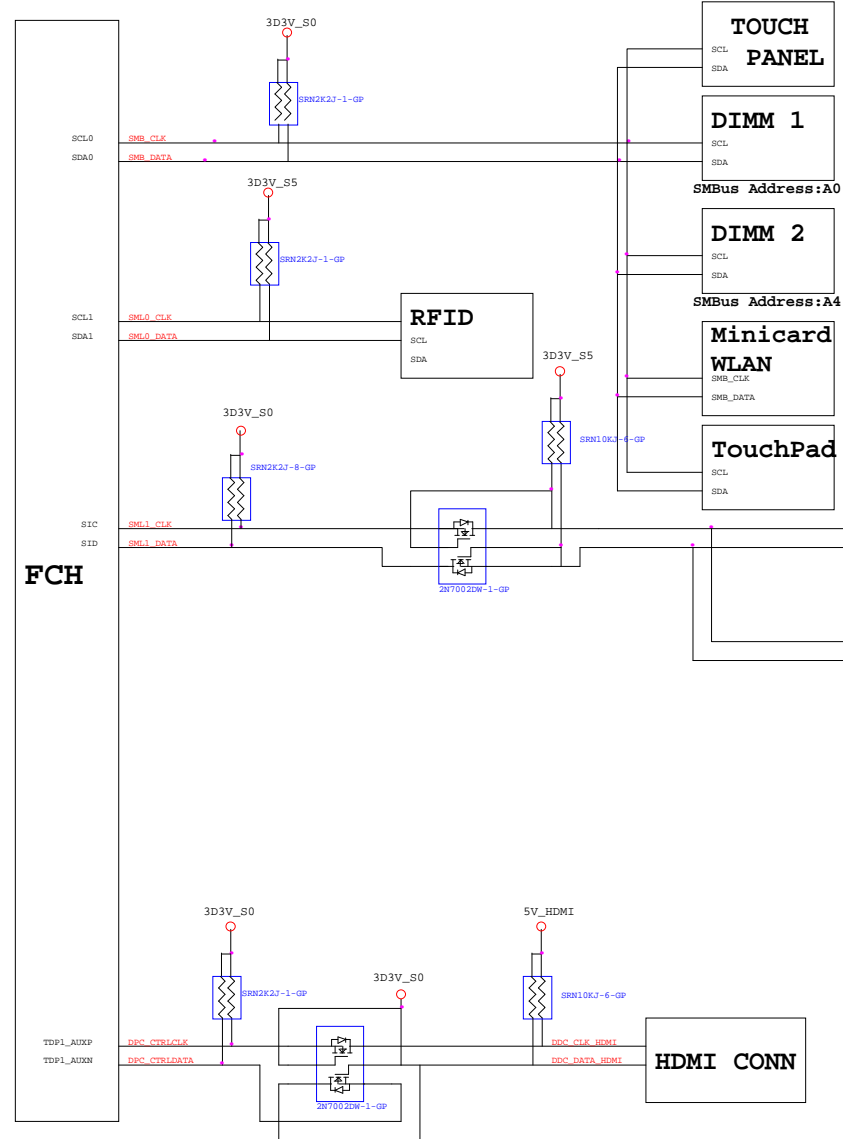
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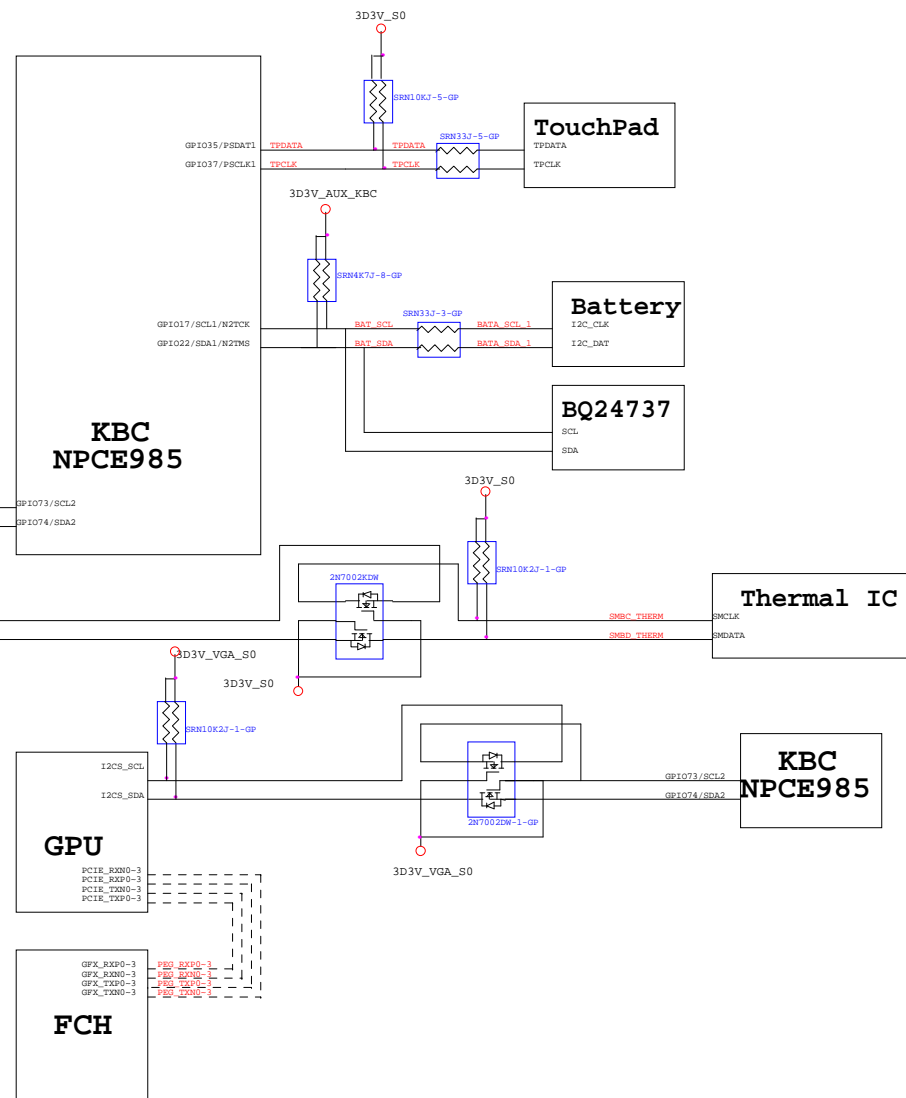




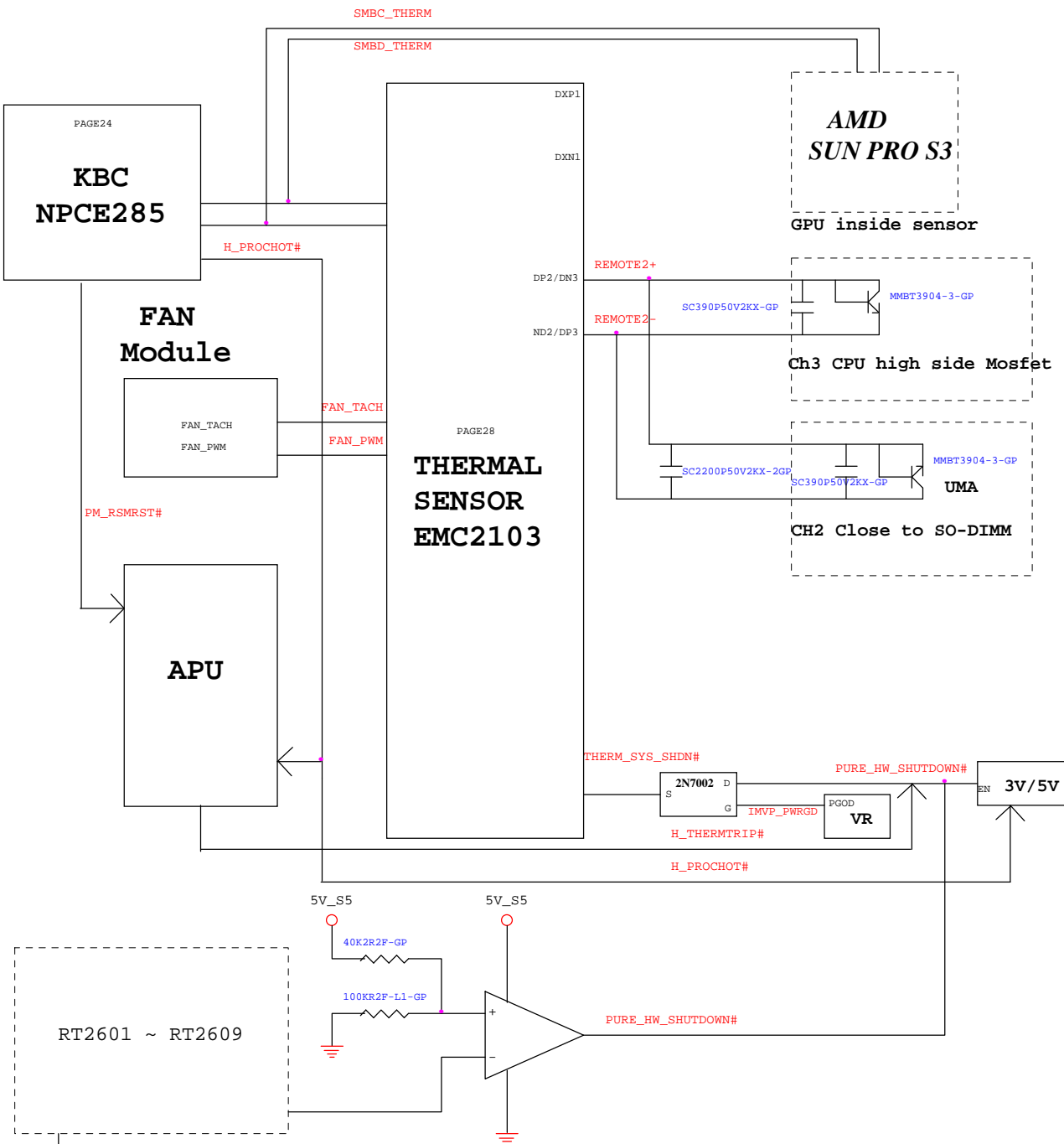
PCH SMBus Block Diagram



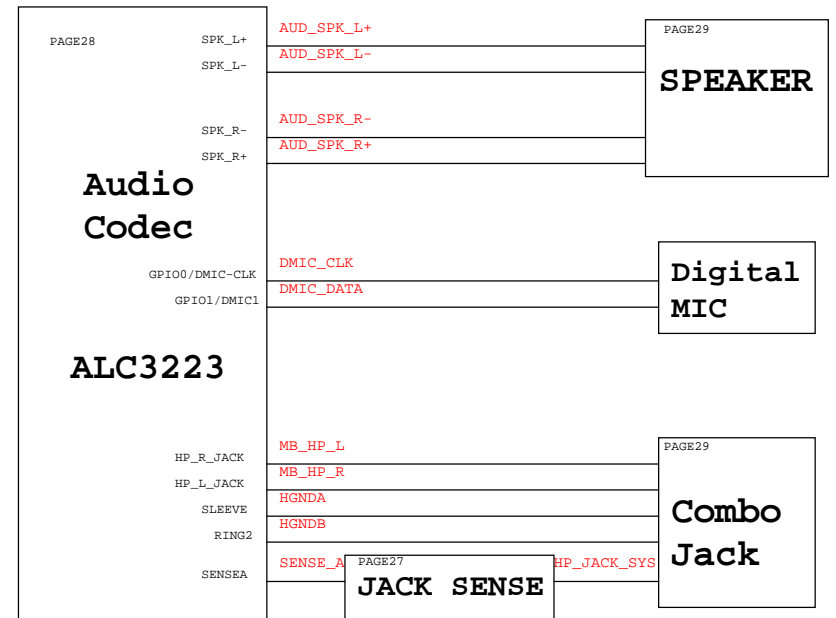
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Change notes -

	VERSION	DATE	Page	Modify List	OWNER
	X01	2013/12/3	83	R8309 = 15Kohm ,C8301/C8313 = DY,C8302 = 1000pF	
	X01	2013/12/3	43 44	RN4301 to 100ohm, AC_IN# change to Pull-H 3D3V_AUX_S5(PR4434)	
	X01	2013/12/3	27	HDA27 change from ALS3223 to ALC3234	
	X01	2013/12/3	24 25	Swap BATT_WHITE_LED# and EC_BRIGHTNESS. BATT_WHITE_LED# to GPIO13 and EC_BRIGHTNESS to GPIO15. Change R2404 from 10K to 20K ohm for PCB VERSION strap , Del SKT25	
	X01	2013/12/3	52	Reserve 0805 0 ohm R5211 between LCDVDD and LCD1.F5201 change from 69.50007.A31 to 69.60040.001	
	X01	2013/12/3	Power	Change C5205,EC4304,EC4601,PC4409,PC4419,PC4511.PC4518,PC4524,PC4720,PC4722,PC4827, PC4913 to 78.10422.2BL (0.1U 25V K0603 X7R) from 78.10424.2BL (0.1U 50V K0603 X7R).	
	X01	2013/12/3	54 55	Add HDMI SMBUS use 0 ohm DUMMY co-lay ,Add Hsync Vsync 0ohm DUMMY co-lay	
	X01	2013/12/3	29	Change HPMIC1 to 022.10002.0001 from 22.10270.G61 SPK1 change to 20.F1639.004	
	X01	2013/12/3	34 63	Change USB1 to 22.10341.Q21 / Change KBLIT1 to 20.K0800.004	
	X01	2013/12/3	19 26	Change C1904 and C1905 from 10pf to 6.8pf / Q2601 RN2602 DUMMY, RN2601 install	
	X01	2013/12/3	30	R3004 CLK_LAN_REQ0#_R change pull high to 3D3V_S0	
	X01	2013/12/3	EMI	DMIC_CLK mount R2716 100ohm resistance,Mount EC9749,Mount EC4304	
	X01	2013/12/3	58	CARD_WLAN_OUT# and CARD_WPAN_OUT# modify to TP change WLAN1 to 62.10043.I81	
	X01	2013/12/3	42 51	DCIN1 change to 20.F1783.007,Del 1D5V_S5 circuit	
	X01	2013/12/4	24 34 35	R2447 change to 63.10334.1DL,Del U3502 and U3501,swap the net U3403.1 and U3403.3	
	X01	2013/12/5	42 46 24 26	Del AFTP3804 AFTP3807, Modify AFTP6241 Add AFTP6242,Change R2447 to 1K , R2622 change to 24.3K	
	X01	2013/12/6	24	R2411 DY D2401 install	
	X01	2013/12/9	31 47 82	RJ45 connector change to 022.10001.0551, PT4701 /PT4704/PT8204 change to 79.3371V.6CL	
	X01	2013/12/10	EMI	Mount EC4303 and change to 0.1u Mount EC9705 EC9748 EC9717 EC9740 EC9741 EC9712 EC9704 EC9708 and change to 0.1u Mount R5415、R5417、R5416、R5414 150ohm resistance Mount TR3401、TR3404、TR6301(69.10103.041、69.10080.011) Mount TR5208、TR5209(69.10103.041、69.10080.011) Mount EC2705、EC2703、EC9739、EC9743、EC9744 0.1u cap Mount SPR2、SPR5、SPR6	
	X01	2013/12/10	0 ohm	change 0 ohm to short pad	
	X01	2013/12/10	54 55	R5501/R5502 change to 33 ohm / Del D5402	
	X01	2013/12/10	24 52 62	R2411 Install D2401 DUMMY ,R5207 BOM control ,BOM control DVC50 to Janus	
	X01	2013/12/12	46 86 62	PR4609 change to 44.2K (64.44225.6DL) from short pad, EMI:Add SPR6(34.42T14.002),KBLIT DUMMY	
	X01	2013/12/16	55 Power	Del HDMI circuit / Modify power schematic BOM	
	X01	2013/12/18	Power	PR8214 change to 499K (64.49935.6DL) / PR8215 change to 9.76K (64.97615.6DL)	

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Taipei Hsien 221, Taiwan, R.O.C.

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	VERSION	DATE	Page	Modify List	OWNER
	X02	2014/01/21	48	Change PR4823 to 26.1K. The voltage about 0.97V	
	X02	2014/01/21	83	R8310 change 15Kohm /C8313 change 0.1uF /C8301 change 470pF Add R8301 for power sequence	
	X02	2014/01/27	12,46	EMC request:change EC4601,C1217,C1225,C1214 to 0.1u	
	X02	2014/01/27		Change 0 ohm to short pad	
	X02	2014/01/27	6	DGPU_PRESENT# pull hi to 3D3V_S0	
	X02	2014/01/28	power	1. PD4201 change 1st source to 83.P6SBM.AAG and 2nd source to 83.P6SBM.DAG . 2. PC4202 PC4409 PC4419 PC4519 PC4524 PC4511 PC4513 PC4518 PC4734 PC4720 PC4722 PC4736 PC4833 PC4827 PC4919 PC4913 PC8230 change to 78.10424.2BL. 3. PC4201 change to 78.10594.41L. 4. PC4916,PC4917 change to 78.10610.5BL. 5. PC4408 change to 78.47522.51L (4.7U 25V K0805 X5R). 6. PC4425 change to 78.10324.2FL (0.01U 50V K0402 X7R). 7. PC4512 change to 78.47522.51L (4.7U 25V K0805 X5R). 8. Delete PC4814/PC4714. 9. Dummy PC4718/PC4912/PC4920/PC4204/PC4205/ PC4426/PC4416/PC4830 10.PC4828 change to 78.47522.51L (4.7U 25V K0805 X5R). 11.PC4909 and PC4911 change to 78.47522.51L (4.7U 25V K0805 X5R).	
	X02	2014/02/06	06 19	Change RN1901 R1901 from short pad to 0 ohm Change RN604 to 66.10336.08L	
	X02	2014/02/06	86	Change SPR4 P/N to 34.15J03.001	
	X02	2014/02/07	26	THM26 DUMMY, Add R2602 for VD_OUT1# connect PURE_HW_SHUTDOWN#	
	A00	2014/02/25		Change PR4911 PR4649 R3016 R6209 R1901 RN5404 RN1901 to short pad	
	A00	2014/02/25	82	Modify schematic PWR_VGA_COMP connecte to PWR_VGA_FB	
	A00	2014/02/25	24	PCB VERSION A/D(PIN98) R2404 change to 64.64925.6DL	